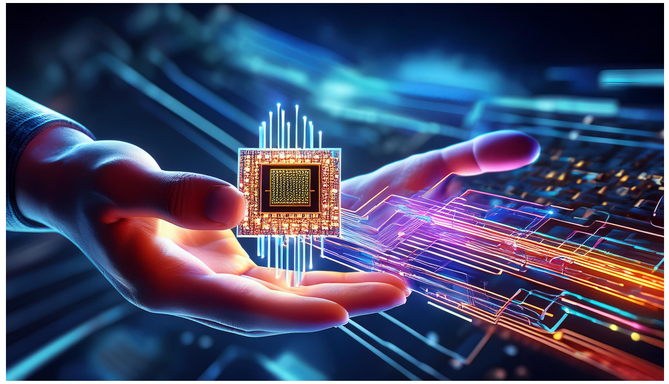
27.09.24 18:00

CSCI 250
Introduction to Computer Organisation
Lecture 2: Computer Memory II



Jetic Gū

2024 Fall Semester (S3)

Overview

- Focus: Course Introduction
- Architecture: Logical Circuits
- Textbook: v4: 8.3; v5: 7.3
- Core Ideas:
    1. SRAM Integrated Circuit
    2. Cache

P1
SRAM

Static RAM Design

P1
SRAM

Static RAM

- SRAMs work by employing latches to store information (typically SR Latches)
- SRAM will hold information permanently unless power is cut
- SRAM uses latches, which requires more components than DRAM so more expensive, but are also much faster
- SRAMs are used in early generations of PCs as main memories, like the VIC-20[1]
- SRAMs now are used as L1 cache, the fasted and smallest cache in CPU
    - Not as fast as registers though due to design restrictions. Register operations usually require a single cycle, L1 cache starts at 2

1. https://en.wikipedia.org/wiki/Static_random-access_memory#:~:text=SRAM was used for the,100, and VIC-20.

Technical

P1
SRAM

Static RAM

- This is a single SRAM cell
- Latches are transparent
    - But RAM doesn't at anytime perform Read/Write simultaneously, so this is less important
- `Select`: like an enabling signal
    - `Select <= 0`, outputs 0 and no inputs are accepted
    - `Select <= 1`, inputs are accepted and outputted

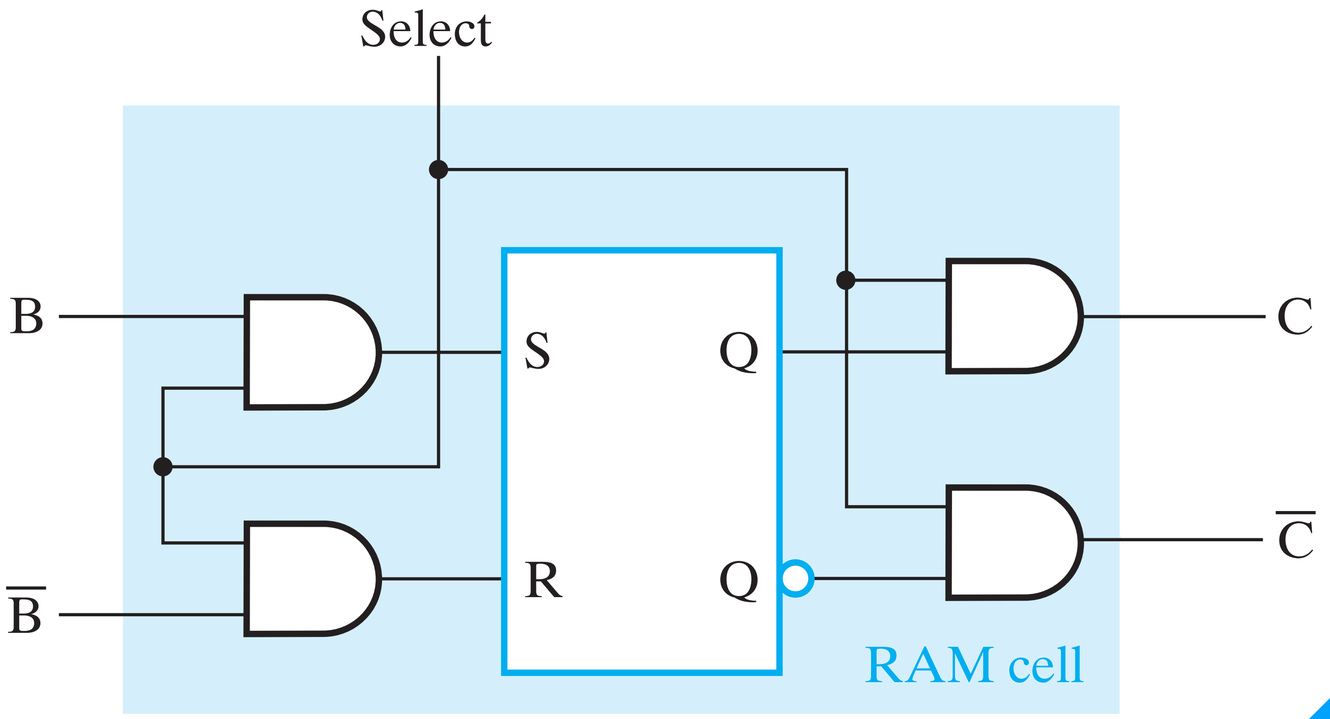


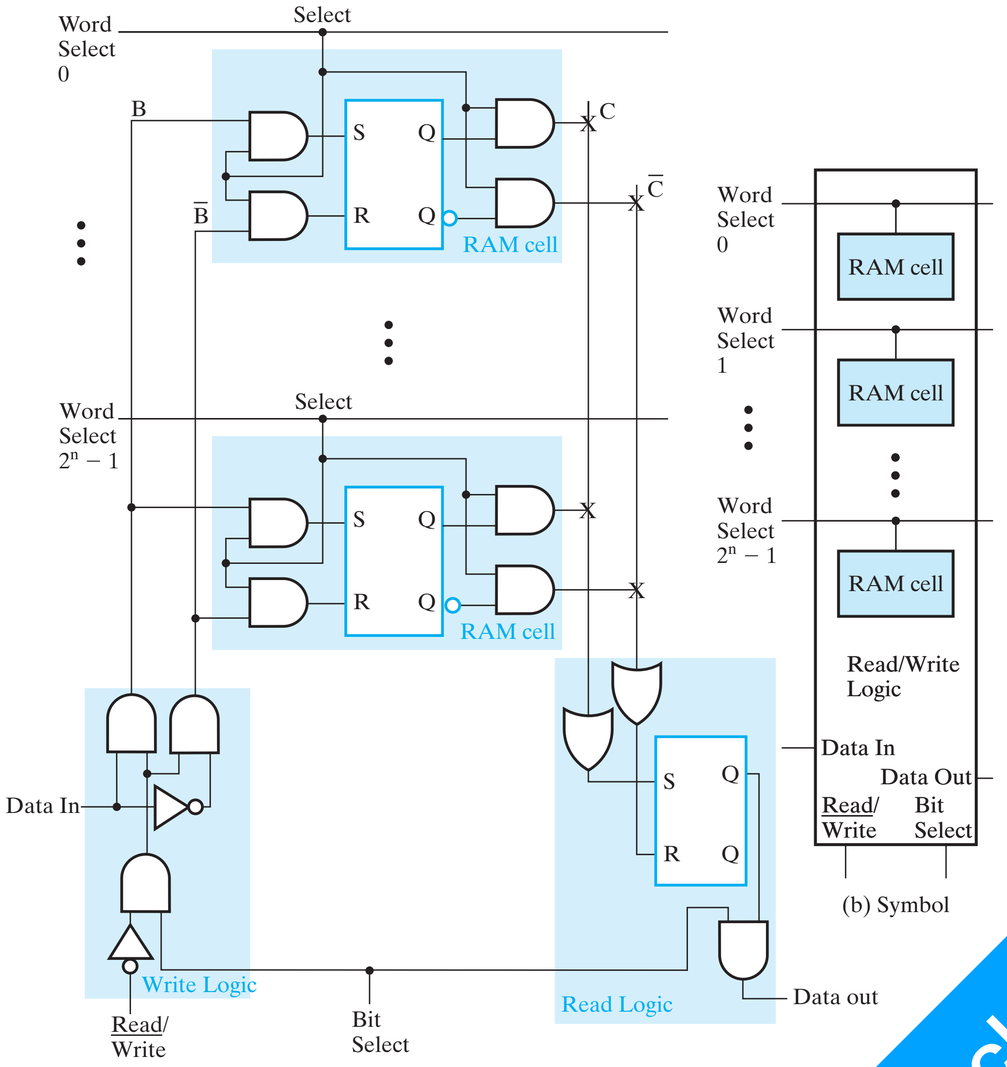
FIGURE 7-4
Static RAM Cell

Technical

P1
SRAM

Static RAM

- This is the diagram for n-bit SRAM
- `Select` signal is shared between all bits of a single word, coming from a decoder
- `Data_in` is combined with `Read/Write` and fed into each n-bit SRAM cells
- `Bit_Select` is like `Chip_Select`/ `Chip_Enable`, for enabling the entire circuit
- The output side are all fed into m-input OR gate

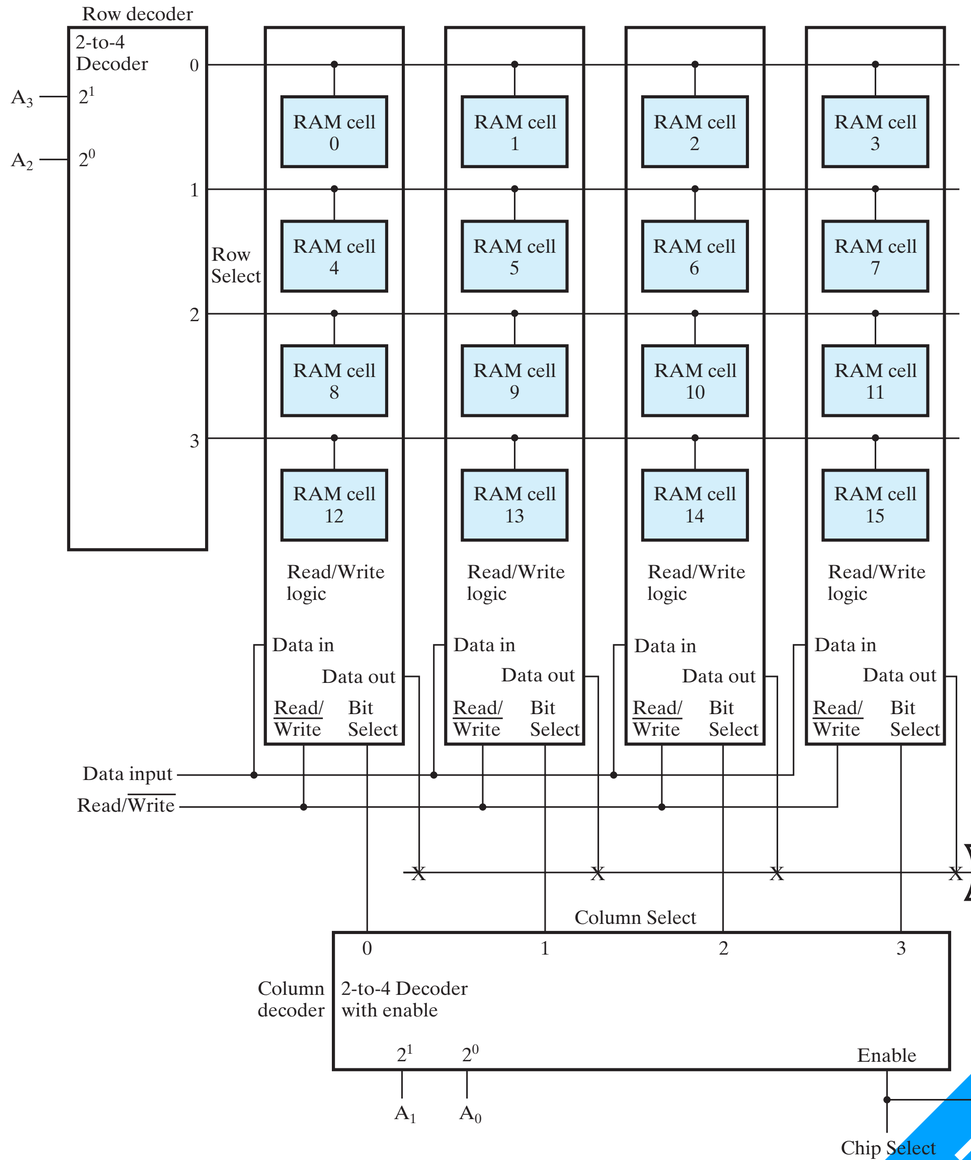


Technical

P1
SRAM

Static RAM

- 16 x 1 RAM Using a 4 x 4 RAM Cell Array
- Row selection and Column selection done separately to avoid more complex decoder designs
    - Also allows the addition of more memory cells easily by the user



Lab 2 Part 1, 2

Lab 2 Part 1

- Create a RAM with the `PROM/RAM wizard` in LogicWorks
  - The RAM unit should support 16bits for address, 16bits for `DI` and `DO`
  - One chip enabling pin is enough
  - Create also a circuit file to test it, make sure you understand how to view/edit the data in the RAM using the `PROM/RAM wizard`

Lab

P2
Lab 2

Lab 2 Part 2

- Create a single SRAM cell using an SR Latch and various gates
  - Inputs: `B`, `nB`, Select; `Output`: `C`, `nC`
  - Save it in your library as `1bit SRAM Cell`
- Create a 4 addresses, 4bit RAM with your SRAM Cells
  - You'll need decoders as well
  - `Data_In`, `Data_Out`: 4bit;
  - `A` (for address): 2bit; `Bit_Select`: 1bit; `R_nW`: 1bit

Lab