Jetic Gū

Columbia College

This assignment is due on 25 July 2022

Please remember to write your name and student number.

You must complete the following assignment and submit a PDF of relevant questions. Handwritten submissions and proprietary formats (e.g. Pages or MS Word) will not be accepted. You will also need to upload LogicWork circuit design file. Then upload a single ZIP file to Moodle.

Submission File structure:

```
submission.zip
    — answer.pdf
    — circuit1-1.cct
    — circuit1-2.cct
    — circuit1-3.cct
    — circuit2.cct
    — circuit3.cct
    — circuit4.cct
    — circuit6.cct
    — circuit7.cct
    — lib.clf
```

The circuit files 1-1, 1-2, 1-3 are 0.5pt each, circuit2 1pt, circuit3 1.5pt, the rest are 2pt each.

!**Important!**: for implementing the sequential circuit, you can use the `D flip-flop wo/SQ` component provided to you, just remember to connect all `R` pins to a single switch input called `Reset`.

# Lab 3

1. Save the library and circuit files we created in class containing the following designs in the final ZIP file:
   A. $D$ latch (`circuit1-1.cct`);
   B. $D$ flip-flop (`circuit1-2.cct`);
   C. Implement $D_A = \overline{X}A + XY$, $D_B = \overline{X}B + XA$, $Z = XB$ (`circuit1-3.cct`);
   D. Draw the state table for 1A (1pt).
2. A sequential circuit has three D flip-flops A, B, and C, and one input X. The circuit is described by the following input equations:

$$D_A = A \oplus B \oplus X$$
$$D_B = A$$
$$D_C = B$$

   A. Derive the state table for the circuit (1pt).
   B. Implement the circuit in logicworks, save as (`circuit2.cct`)

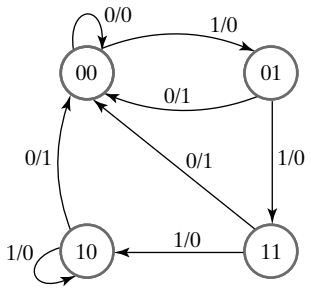
3. You are tasked to design a 3bit counter, the counter will have three D Flip-Flops $A_2$, $A_1$, and $A_0$, for every single CLK pulse, its value increases by 1. Say at time 0, $A_2A_1A_0 = 000$, then the next time step it should be $001$, and the next $010$, so on.

   A. Assuming the next states are $D_2$, $D_1$, and $D_0$, derive the state table for the circuit (1pt).

   B. Perform optimisation, find the optimised boolean expressions for $D_2$, $D_1$, and $D_0$ (1pt).

   C. Implement the circuit in logicworks, save as (`circuit3.cct`)

4. For the following state diagram.

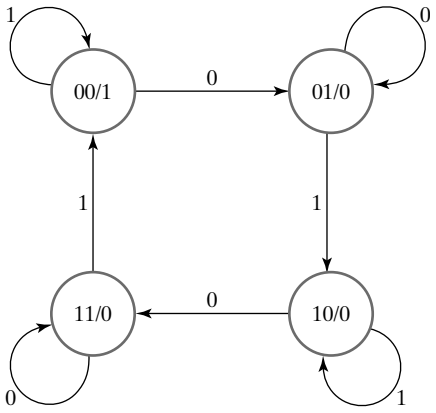



   A. Starting from state 00 in the following state diagram, determine the state transitions and output sequence that will be generated when an input sequence of 10011011110 is applied (1pt).

   B. Draw the state table, perform flip-flop input equation determination and output equation determination (1pt).

   C. Implement the circuit in logicworks as (`circuit4.cct`)

5. A sequential circuit has two flip-flops $A$ and $B$, one input $X$, and one output $Y$. The state diagram is shown in the following figure. Draw the state table, and perform 1-hot state assignment (1pt).




6. Draw the state diagram of rotator, write down the equations for each $D$ flip-flop (1pt), and complete the implementation (`circuit6.cct`).

**Start state** $X_3X_2X_1X_0$: original 4-bit, implement using binary switches

**Input** $Y$

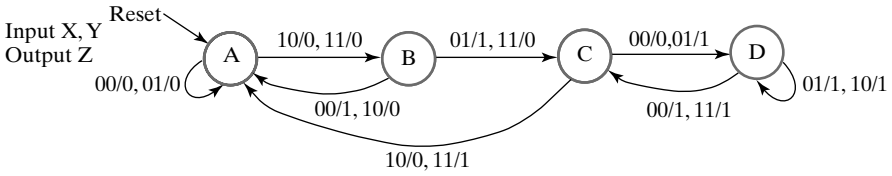
0: for left rotation (output $X_2X_1X_0X_3$);

1: for right rotation (output $X_0X_3X_2X_1$);

**Behaviour**

Every CLK triggers a shift

7. Find a state-machine diagram that is equivalent to the following state diagram. Reduce the complexity of the transition conditions as much as possible. Attempt to make outputs unconditional by changing Mealy outputs to Moore outputs. Make a state assignment to your state-machine diagram and find an implementation for the corresponding sequential circuit using $D$ flop-flops, AND gates, OR gates, and inverters.




(1) Draw the state-machine diagram (1pt).

(2) Write down the Flip-Flop Input Equations and Output Equations (1pt).

(3) Implement the circuit, save as `circuit7.cct` .