Name		Quiz Date	2021.11.01
Student #		Time	Due 11.07
Mark		Full Mark	30pt

01.11.21 11:51

Please remember to write your name and student number. Calculators are not allowed. The consequences of cheating will be severe. Please submit a single PDF. Handwritten submissions and proprietary formats (e.g. Pages or MS Word) will not be accepted. For circuit diagrams, use LogicWorks and attach screenshots here.

Midterm

1. (5pt) Multiple choice questions

   I. What does bitrate mean?

      A. Number of cycles per second

      B. Number of samples per second

      C. Number of samples per cycle

      D. Number of digital bits per second

   II. Which of the following is NOT in 5-step systematic design procedure?

      A. Formulation

      B. Optimisation

      C. Technology Mapping

      D. None of above

   III. Which of the following statements is false?

      A. Analog circuits cannot process digital information

      B. Digital circuits cannot process analog signals

      C. Analog circuits are less resistant to noise and interference than digital circuits

      D. None of above

   IV. What is ASCII used for?

      A. Represent strings in digital circuits

      B. Represent 2s complement in digital circuits

      C. Represent integers in digital circuits

      D. Represent hexadecimal numbers in digital circuits

   V. Which of the following may NOT be an advantage of hierarchical design?

      A. Ability to reuse designed components

      B. Reduce overall delay

      C. Simplify design complexity

      D. Easier verification and debugging

2. (5pt) Representations of numbers: 12, 35

   A. Write down the values in Binary, Octal, and Hexadecimal systems

   B. Represent the values as 8-bit unsigned integers, with the first bit for odd parity

   C. Represent the values in BCD

   D. Represent the values as 8-bit signed integers, also write down their unsigned 2s complements

   E. Treating the numbers as strings, write down their ASCII code

3. (5pt) Boolean algebra

   A. Prove using truth table: $X + \overline{Y} + \overline{Z} = \overline{\overline{X} Y Z}$

   B. Convert to Sum-of-Minterm: $F(X, Y, Z) = XY + YZ$

   C. Simplify using algebraic manipulation:
   $(A + B + C + D)(A + B + C + \overline{D})(A + B + \overline{C})(A + \overline{B})$

   D. Simplify using K-map: $F(A, B, C) = \Sigma m(0,2,4,5,6,7)$

   E. Simplify using K-map with don't care conditions: $F(A, B, C, D) = \Sigma m(0,5,7,8,10,13)$,
   $d(A, B, C, D) = \Sigma m(2,4,14,15)$

4. (5pt) Design a circuit to implement the following pair of Boolean equations:

$$F = (A + (C + D)(\overline{C} + E))(\overline{A} + D)$$
$$G = (B + (C + D)(\overline{C} + E))(\overline{B} + C)$$

To simplify drawing the schematic, the circuit is to use a hierarchy based on the factoring shown in the equation. Three instances (copies) of a single hierarchical circuit component made up of two OR gates, an AND gate, and an inverter are to be used. Draw the logic diagram for the hierarchical component and for the overall circuit diagram using a symbol for the hierarchical component.

5. (5pt) With a single 1 bit 8-to-1 multiplexer (8channel 1bit Multiplexer) and no other gates, implement the following sum of minterm: $F(X, Y, Z) = \Sigma m(1,2,6,7)$.

6. (5pt) Implement signed 2s complementor

   A. A signed 2s complementor is different from an unsigned one, in which if the sign bit of input X is 0, the signed 2s complement of X is X. If the sign bit of X is 1, the signed 2s complement of X will be the unsigned 2s complement of X, with sign bit equals 1. Draw the truth table for a 4-bit signed 2s complementor (2pt)

   B. Design a 4-bit signed 2s complementor in LogicWorks, attach screenshots here. (3pt)