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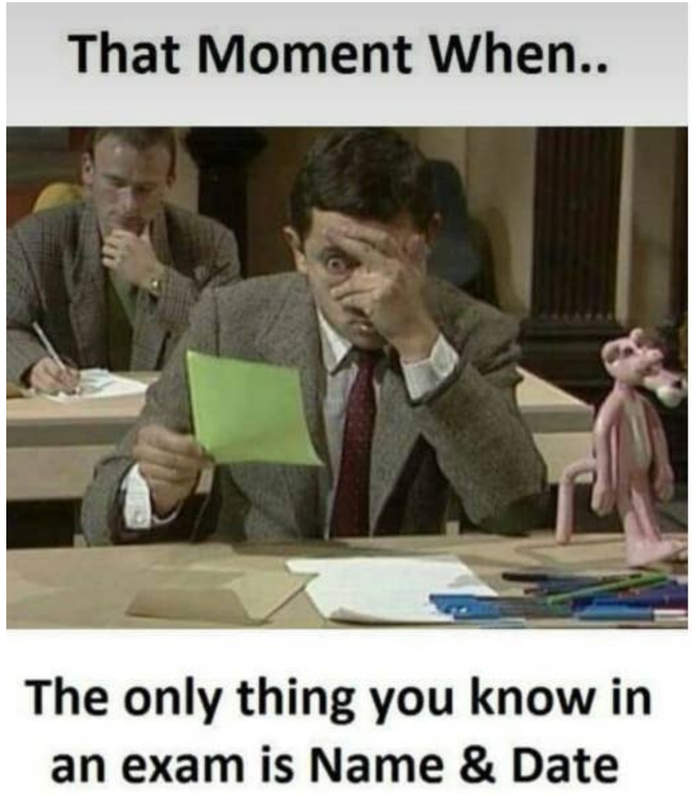
CSCI 150
Introduction to Digital and Computer System Design
Final Review Week

Jetic Gū

2021 Summer Semester (S2)



Overview

- Focus: Reviews
- Architecture: von Neumann
- Core Ideas:
    1. Information about the Final Exam, and the Final Review week
    2. List of all the materials we've covered

P1
Information

Final Exam

- 10 Aug 2021, 17:30-20:30 (3 hours)
  - Actual load: **2 hours**
  - Website opens: 17:**25**-20:**35**
- Questions **required** to be submitted on the test website
- Questions **required** to be submitted on Moodle (PDF)

Lecture Mon 12:00-13:50; Wed 12:00-12:50; Thur 12:00-13:50	**Location**: Online using Zoom Columbia College Main Campus
Office Hour Mon 11:00-12:00; Online	**Midterm** 5 July 2021, 12:00-13:50 (Online) **Final** 10 Aug 2021, 17:30-20:30 (Online)

Concept

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Information

Final Exam

- This Thursday/Tomorrow: 2 hour office hour, no actual class
- You do **NOT** need to live-stream yourself doing the test

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Information

Final Exam

- College Policy
  - Closed-Book Exam (like any of us cares)
  - Sick/Absence: email me for deferral, I will submit to the counsellor
    - Retake/Make up: determined by the counsellor, he/she will contact you

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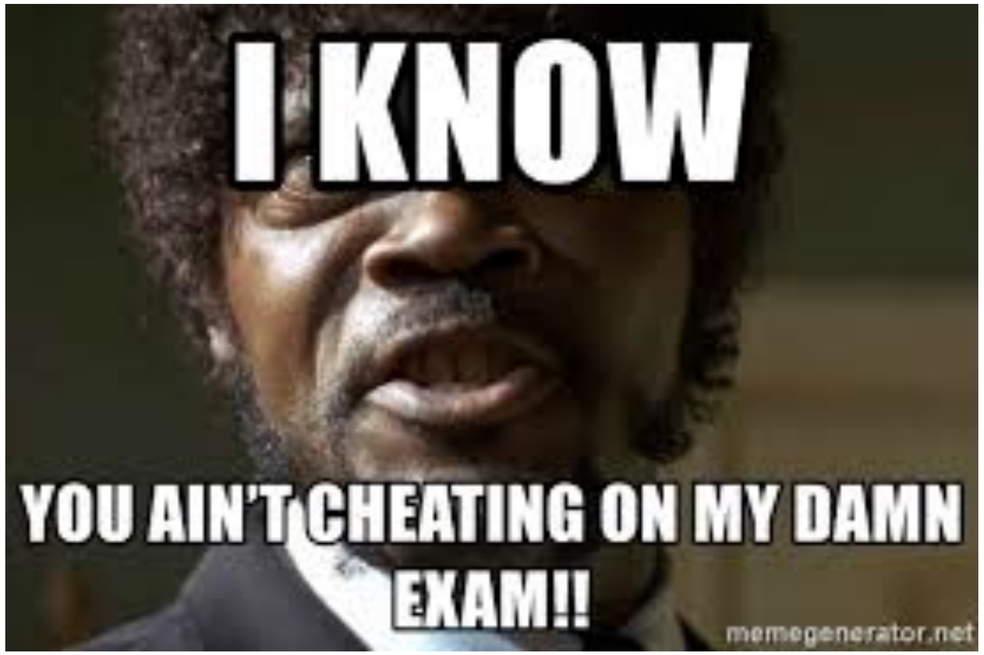
Information

Final Exam

- College Policy
  - Cheating
    Me: **report** to the Academic Board
    You: **expelled** and **ejected** into the **sun** (or just where you came from)



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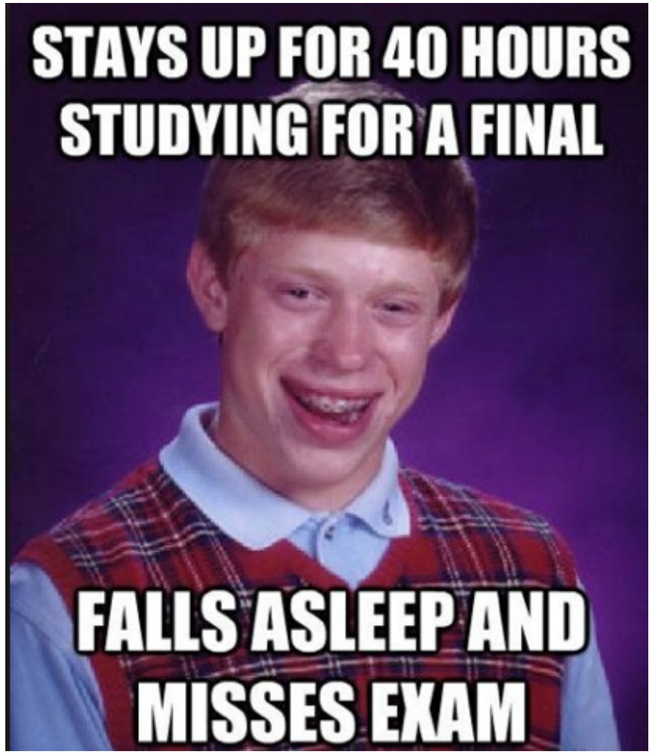
Information

Most Importantly…

- Stay **Healthy**
- Stay **Active**
- Be **Positive**
- **DO NOT STAY UP LATE**



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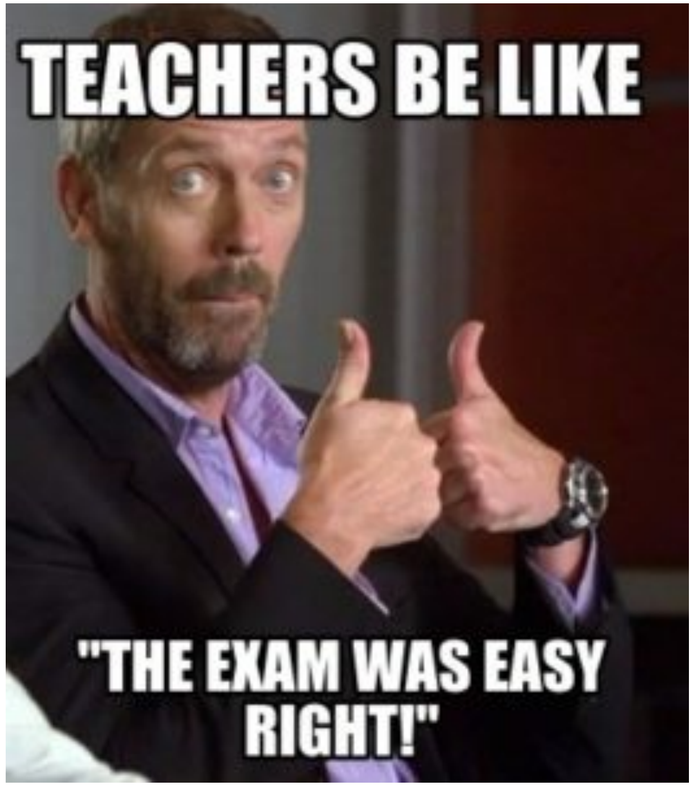
P2
Final Review

Recap:
what we've done



Summary

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Final Review

Lecture 1

- **LS01**: Analog vs Digital; von Neumann Architecture; Embedded System; Binary, Octal, Hexadecimal Systems
- **LS02**: Arithmetic (+, -, ×); Unsigned vs Signed Integers; Digital/Analog Conversion
- **LS03**: BCD, ASCII, Parity Code

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Final Review

Lecture 2

- **LS04**: AND/OR/NOT gates; Gating Delay; Boolean Algebra; Truth Table; Simulation & Timing Diagram;
- **LS05**: Binary Identities; Algebraic Manipulation; Complementation;
- **LS06**: Minterm/Maxterm; Sum-of-Products, Product-of-Sums;
- **LS07**: K-Map; Don’t Care conditions
- **LS08**: XOR; Buffer and Other Gates; Propagation/Transfer/Inertial Delay; Standard Load;

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Lecture 3A

- **LS09**: 5-Step systematic designing procedures
- **LS10**: Technology Mapping; Hierarchical Design; Functional Blocks
- **LS11**: Value-Fixing; Transferring; Inverting; Enabler; Decoder; Vector Denotation
- **LS12**: Encoder; Priority Encoder; Multiplexer

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Lecture 3B

- **LS13**: 1-bit Half Adder; 1-bit Full Adder; n-bit Full Adder (Ripple Carry)
- **LS14**: Unsigned 1-bit Subtractor; Unsigned n-bit Subtractor
- **LS15**: Unsigned 2s complement; Unsigned Subtractor correction; Adder-Subtractor; Simple Adder-Subtractor
- **LS16**: Overflow; Signed 2s complement; Signed Arithmetics; Incrementing/Decrementing; Zero Filling/Extension; Multiplication/Division by Constants

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Lecture 4

- **LS19**: Sequential Circuit; Stability; SR Latch; D latch
- **LS20**: Master-Slave Flip-Flops; D Flip-Flop
- **LS21**: State Table
- **LS22**: State Diagram (Mealy); 8-Step Design Procedures
- **LS23**: State Assignment; Input/Output Equation Determination; Unused States
- **LS24**: State Machine Diagram (Moore); TC and OC

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Lecture 5

- **LS26**: Registers; Datapath; Loading/Clearing/Enabling; GPR; Microoperations
- **LS27**: Datapath Implementation; Selecting Register; Datapath-level microoperation Implementation
- **LS28**: Single Register Microoperation Implementation; Multiple Register Microoperation Implementation
- **LS29**: How to implement a datapath
- **LS30**: Register Cell Design; Ripple Counter; Synchronous Counter; BCD Counter

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Q&A Time

Happy Review Week