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This assignment is due on 12 Feb. 2021

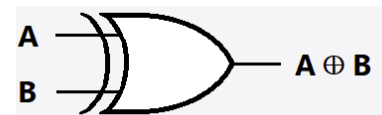
Please remember to write your name and student number.

Please submit a single PDF for each assignment. Handwritten submissions and proprietary formats (e.g. Pages or MS Word) will not be accepted. The Lab portion must be submitted separately.

Assignment 2

- Prove the following boolean equations.
 - Using truth table, DeMorgan's theorem for four variables: $\overline{ABCD} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$
 - Using algebraic manipulation: $A(\overline{A} + B)(\overline{A}\overline{B} + C)(\overline{A}\overline{B}\overline{C} + D) = ABCD$
 - Using algebraic manipulation: $\overline{X}Y + \overline{Y}Z + X\overline{Z} = X\overline{Y} + Y\overline{Z} + \overline{X}Z$
- Optimise the following boolean functions using a K-map.
 - $F(A, B, C, D) = \Sigma m(2,3,8,9,10,12,13,14)$
 - $F(A, B, C, D) = \Sigma m(1,3,6,7,9,11,12,13,15)$
- Optimise the following boolean expressions in Product-of-Sums form.
 - $F(A, B, C, D) = \Sigma m(0,2,3,4,8,10,11,15)$
 - $F(W, X, Y, Z) = \Pi M(0,2,4,5,8,10,11,12,13,14)$
- The denotation of don't care condition is $d(A, B, C, D) = \Sigma m(\dots)$ complementing the boolean function F . Optimise the following Boolean function F together with the don't care condition d .
 - $F(A, B, C, D) = \Sigma m(0,1,7,13,15)$, $d(A, B, C, D) = \Sigma m(2,4,6,8,9,10)$
 - $F(A, B, C) = \Sigma m(1,2,4)$, $d(A, B, C) = \Sigma m(0,3,6,7)$
- An exclusive-OR (XOR, \oplus) gate is a gate with the following truth table:

X	Y	$X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0



- Write down the boolean expression of XOR in sum-of-products and product-of-sums.
- Draw the circuit diagram implementation with AND, OR, NOT gates for XOR.

Lab 1

You must complete the following assignment and submit a PDF of instructions enough to replicate your results, and required documentation. You will also need to upload LogicWork circuit design file. Then upload a single ZIP file to student portal.

1. You are having a wonderful day in the park. Suddenly the park manager finds you and tells you the sad story of how his lock got broken and now he needs a new lock for his shed. Your task is to design such a lock using digital circuit. The lock has one binary output named `LOCK`, when its value is 0 it is locked, 1 it is unlocked. The input is the combination, denoted by 6 binary switches (named `s1`, `s2`, ..., `s6`). The lock is unlocked only when the combination matches 101110.
 - A. Draw the truth table of this digital circuit, write down the boolean expression.
 - B. Implement the digital circuit in LogicWorks. Save the file as `circuit1_1.cct`.
 - C. The park ranger out-of-the-blue, decides to give his girlfriend a different combination that can also unlock it. The new combination is 010101, both combinations should be able to unlock it. Draw the new truth table, write down the boolean expression.
 - D. Implement the new circuit in LogicWorks. Save the file as `circuit1_2.cct`.
 - E. Write down boolean expression implementing the OR gate using XOR, AND, and NOT gates.
 - F. The park ranger just informed you that he hates OR gates and wants the new circuit designed with AND, XOR, and NOT gates only. Implement the new circuit in LogicWorks, save the file as `circuit1_3.cct`.

2. We discussed the scenario of designing a curtain motor control unit in class, with 2 sensors (represented using binary switches), 2 motors and a LED light (represented using just binary prob), and 2 buttons (represented using binary switches). If you don't remember what this is, go through the slides in `#04-2020-1002-104_Lecture2_Combinational_Logical_Circuits_I`.
 - A. Draw the truth table of this digital circuit.
 - B. Implement the digital circuit in LogicWorks. Save the file as `circuit2.cct`.