

CSCI 150 Introduction to Digital and Computer System Design Lecture 2: Combinational Logical Circuits I



Jetic Gū 2020 Fall Semester (S3)

Overview

- Focus: Boolean Algebra
- Architecture: Combinatory Logical Circuits
- Textbook v4: Ch2 2.1 2.2; v5: Ch2 2.1 2.2
- Core Ideas:
 - 1. Logical Gates
 - 2. Introduction to LogicWorks

Logic Gates

And, Or, Not Gates, LogicWorks

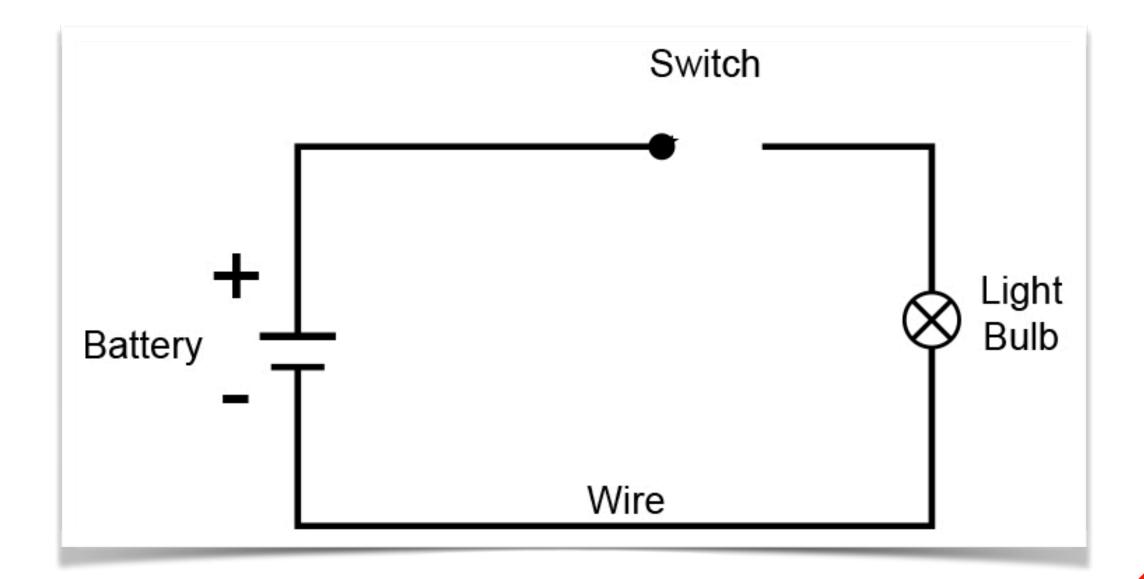
What is a Logic Gate?

- A basic circuit unit implemented using transistors and interconnections
 - We when analysing a digital circuit, are not concerned with the internals of a gate, but only it's external properties
 - Performs a single logical operation
 operate on one or more binary input signals to produce an output signal

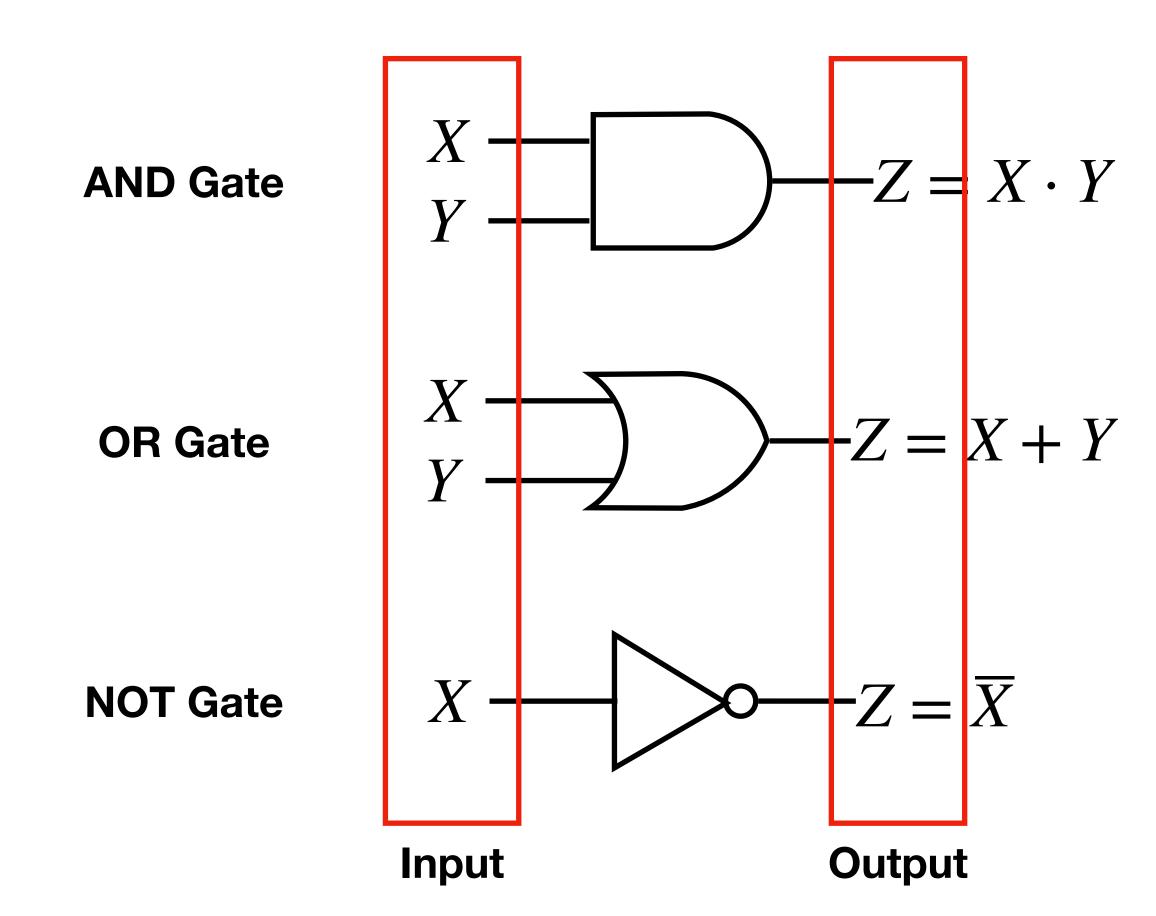
Color

What is a Logic Gate?

- Similar to in electric circuit design, we are not concerned with the design of the lightbulb or battery, but we know what it does.
- A logic gate is like that, we know it's external logic properties, that's enough.

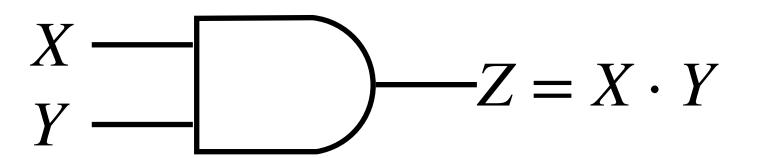


First 3 Gates



P1 Logic Gates

AND Operator and Boolean Algebra / Binary Logic



- Boolean Algebra
 - Each variable can only have one of two values:
 - TRUE/ON/1
 - False/OFF/0
- ullet AND: Z is equal to X AND Y
 - Operator: · (\cdot)

Color

AND Operator and Boolean Algebra

$$X \longrightarrow Z = X \cdot Y$$

AND Truth Table

X	Y	$Z = X \cdot Y$
0	0	0
0	1	0
1	0	0
1	1	1

- ullet AND: Z is equal to X AND Y
 - Operator: · (\cdot)
- Truth Table
 - Left: all combinations of input values
 - Right: corresponding output values

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OR Operator

$$X \longrightarrow Z = X + Y$$

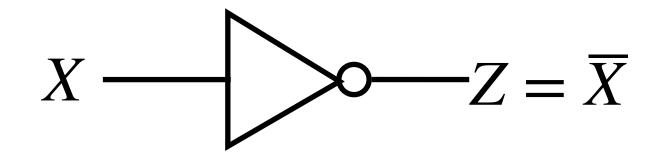
OR Truth Table

X	Y	Z = X + Y
0	0	0
0	1	1
1	0	1
1	1	1

ullet OR: Z is equal to X or Y

Operator: +

NOT Operator



OR Truth Table

X	$Z = \overline{X}$
0	1
1	0

- ullet NOT: Z is equal to NOT X
 - Operator: \overline{X} (\overline {X})
 - Also called: Complement operation; Inverter gate

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Logic Gate and Boolean Algebra

- Logic Gates
 - AND Gate, OR Gate, NOT Gate
 - Actual physical components

- Boolean Algebra Operators
 - AND (·), OR (+), NOT (\overline{X})
 - Mathematical Representations

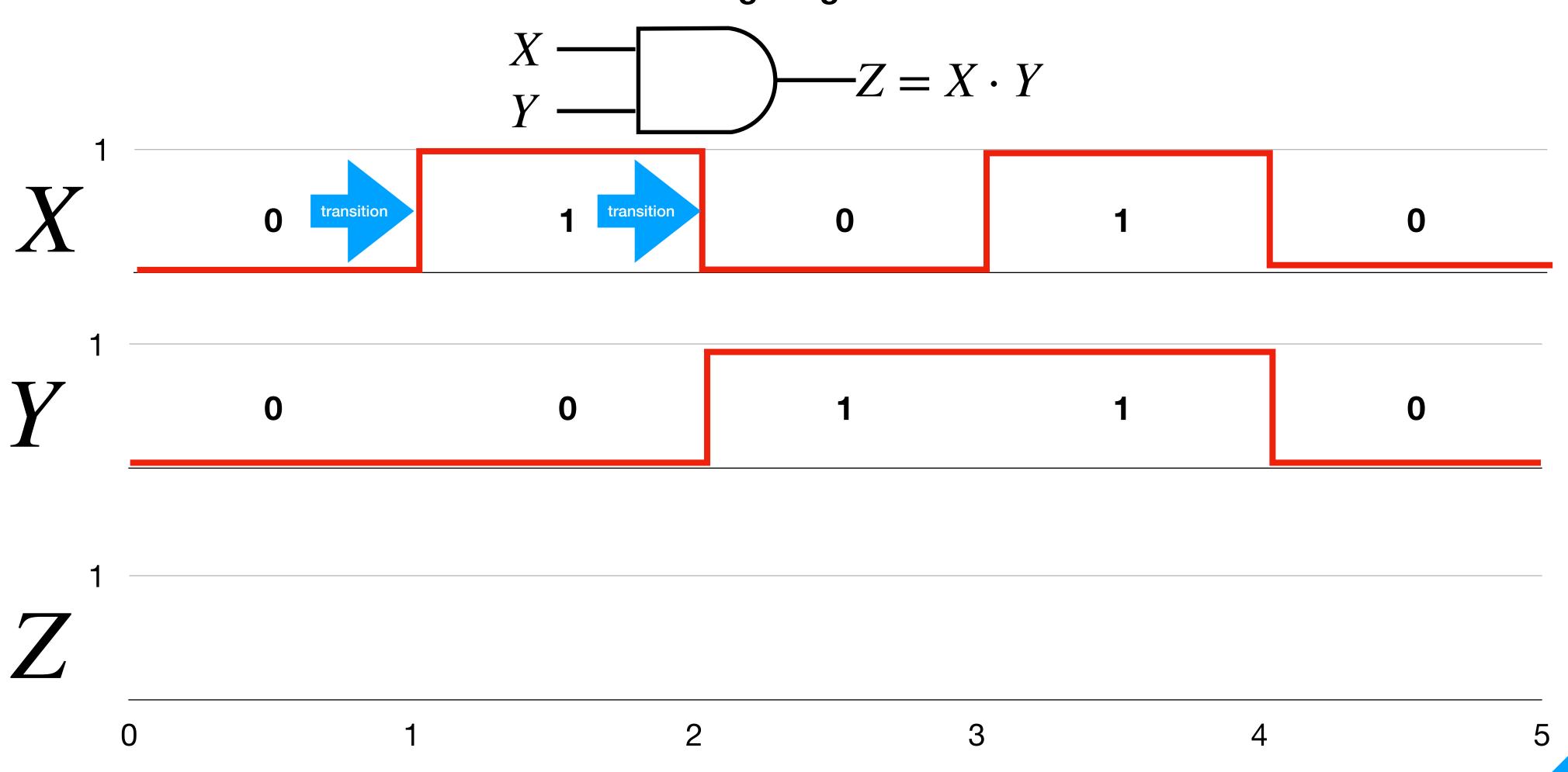
THEY HAVE
DIFFERENCES!

Digital Logical Gates

- In math, everything happens simultaneously
 - An equation like 250 + 760 = 1010 doesn't change with time/location
- In digital circuits, we have **electrons as 'messengers'**. They travel at about 2,200 kilometres per second
 - Logic gates are tiny circuits, which means they still have internal components: even slower
 - This means: there will be tiny delays called Gate Delay

Digital Logical Gates

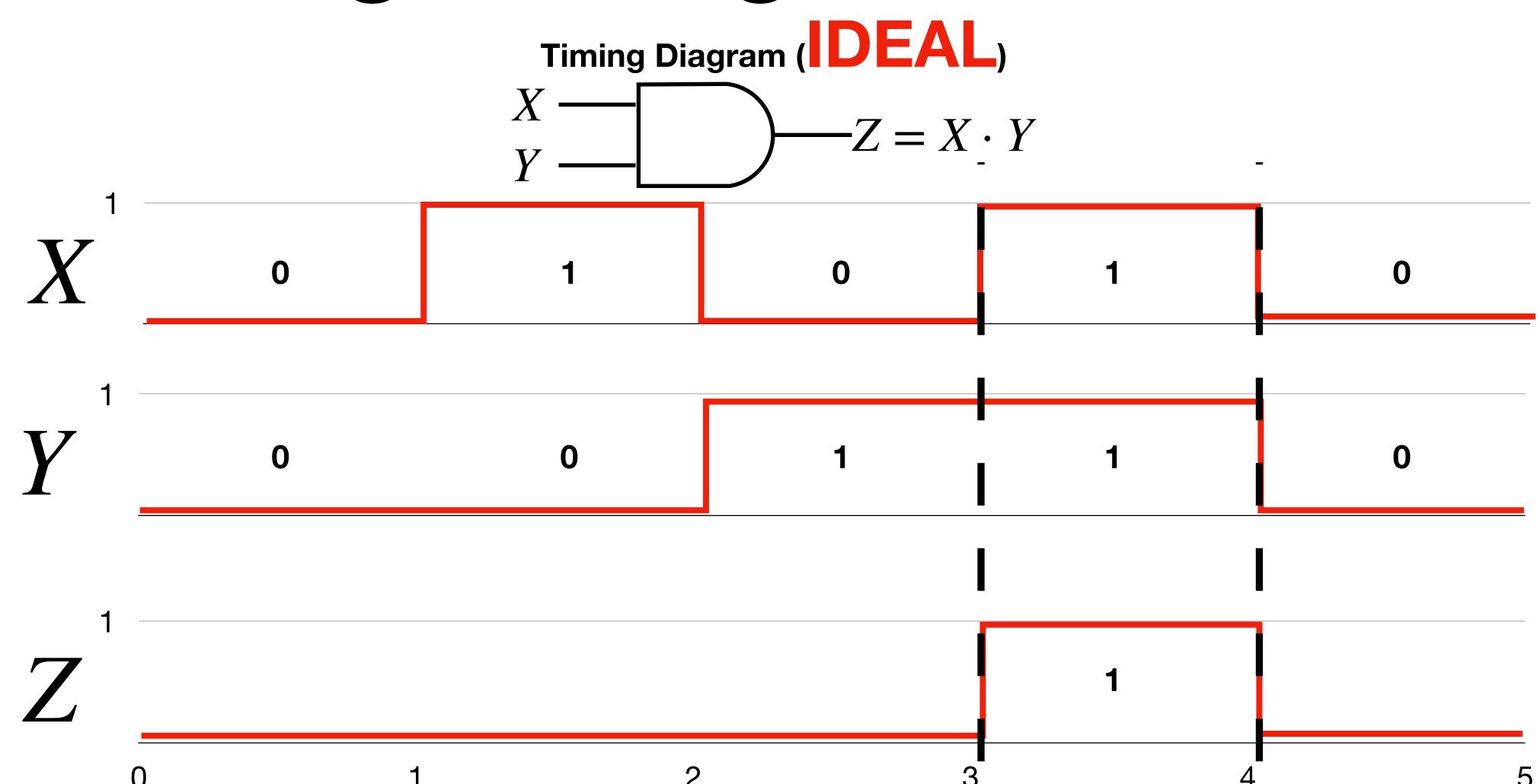
Timing Diagram



Chilico

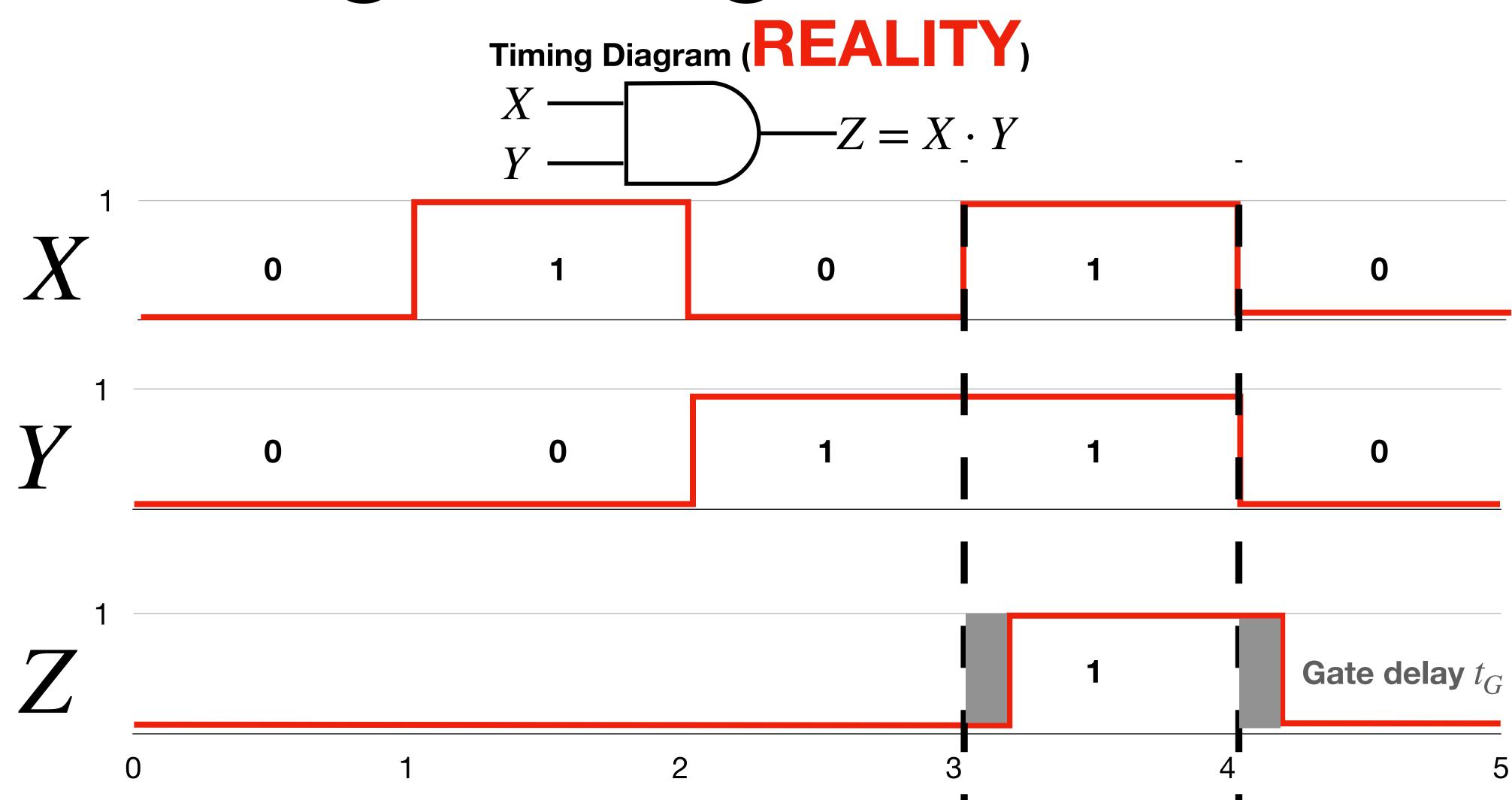
P1 Logic Gates

Digital Logical Gates



P1 Logic Gates

Digital Logical Gates



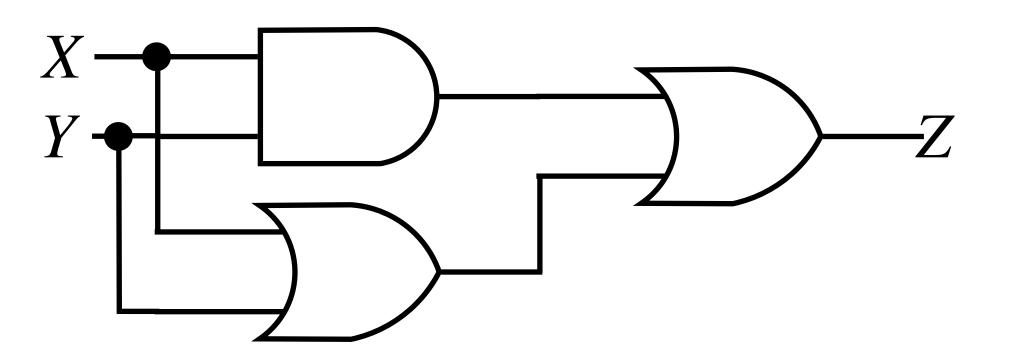
Gate Delay

- Gate delay are small, but not ignorable in practice
 - for simulation, you can ignore it for now
- Gate delay differs for different types and implementations of Gates

Simulation 1



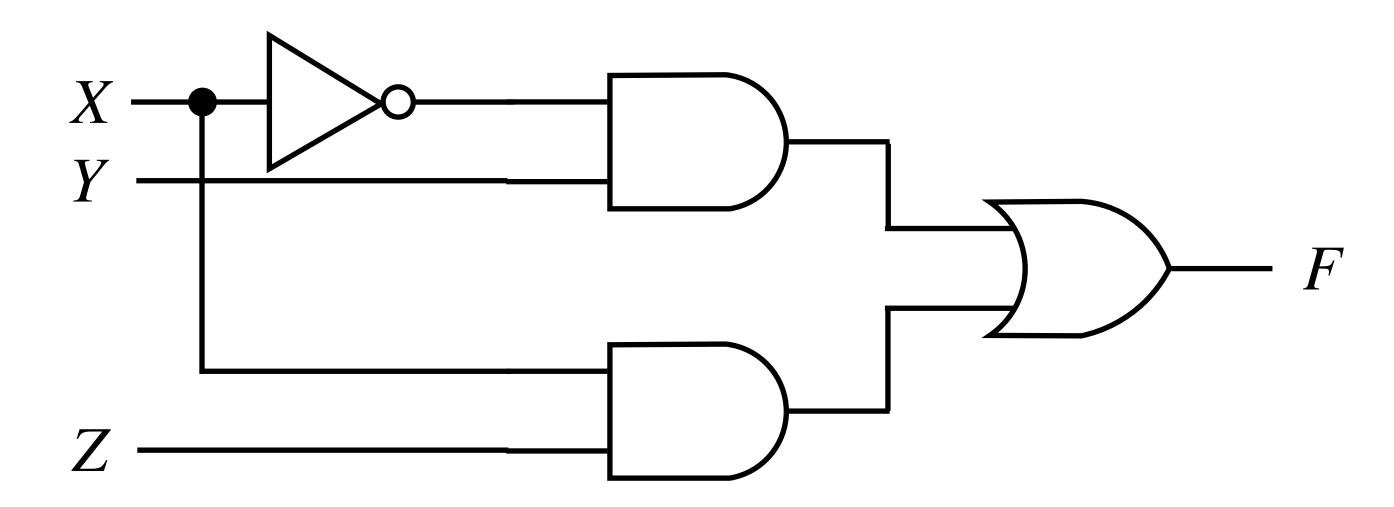
X	Y	$Z = (X \cdot Y) + (X + Y)$
0	0	
0	1	
1	0	
1	1	



Simulation 2



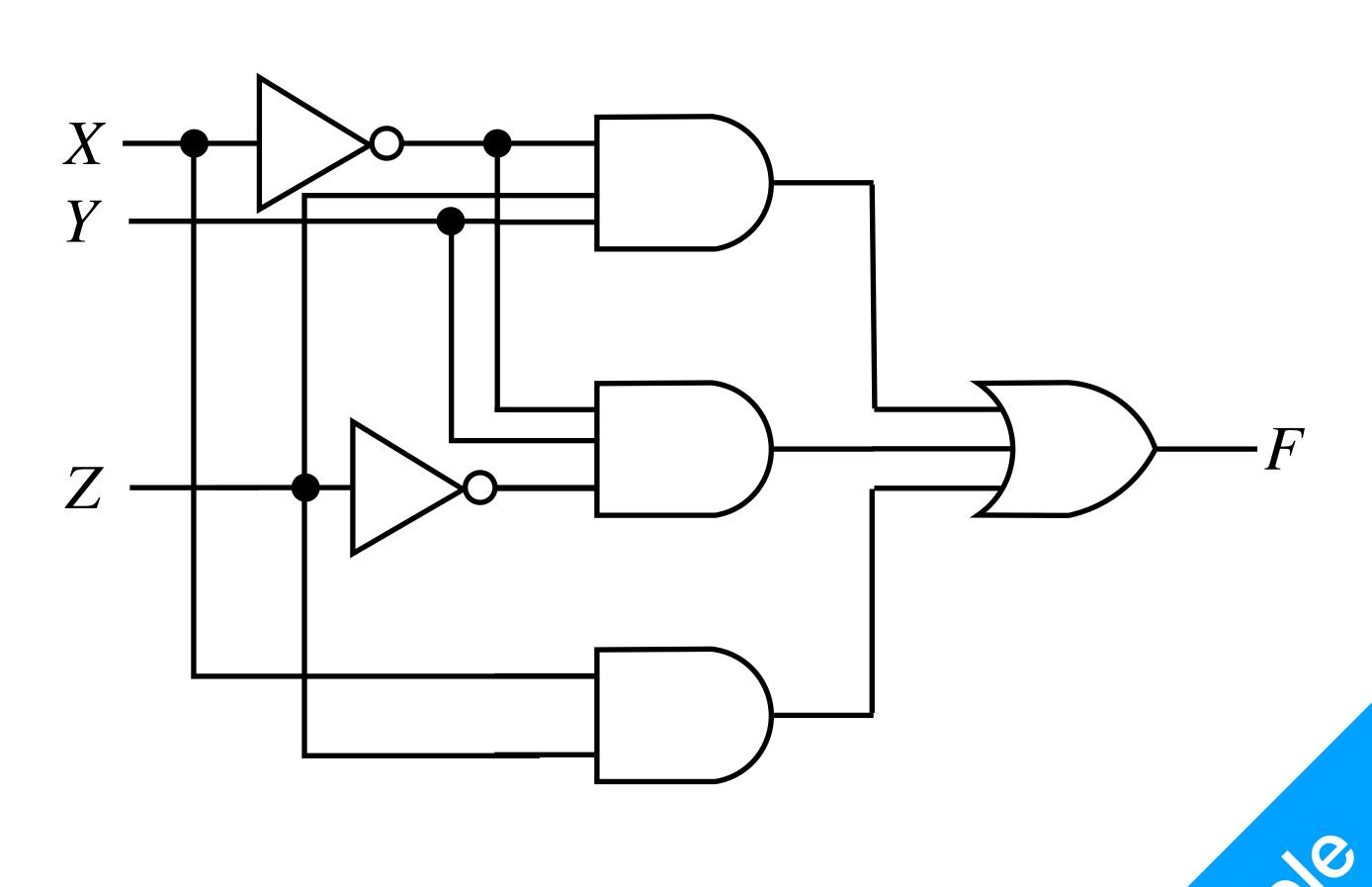
X	Y	Z	$F = (\overline{X}Y) + (XZ)$
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	



Simulation 3



X	Y	Z	$F = \overline{X}YZ + \overline{X}Y\overline{Z} + XZ$
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1		

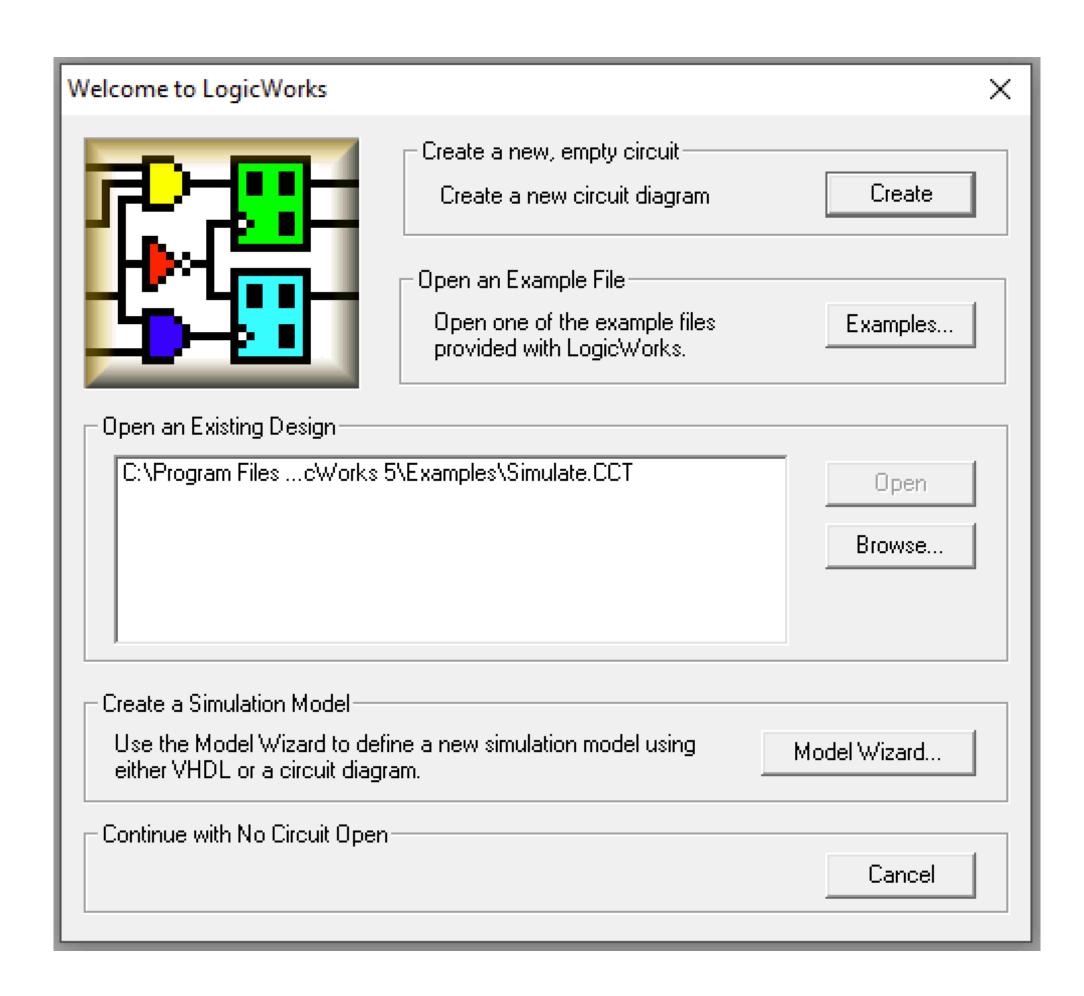


Summary

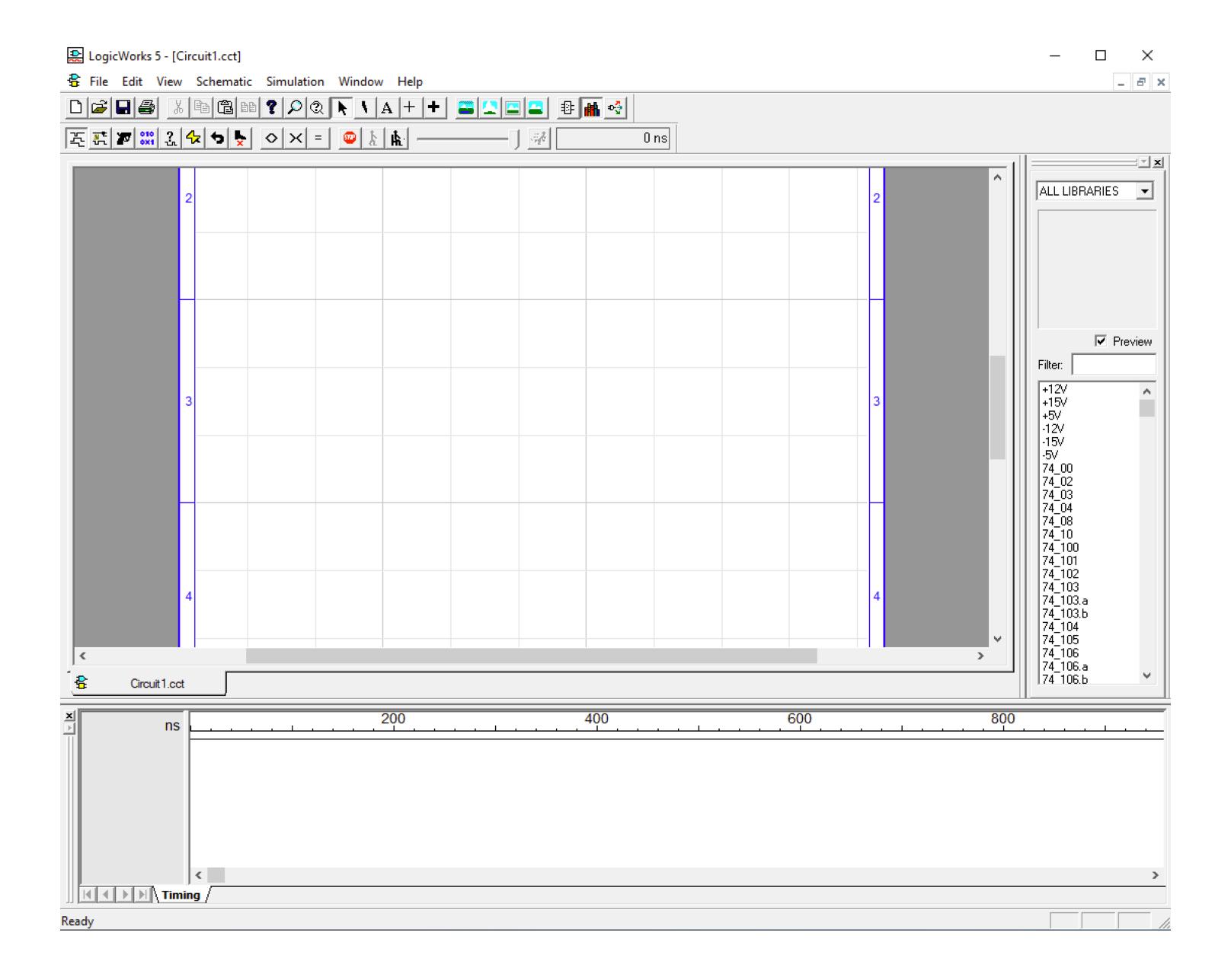
- AND, OR, NOT Operators
- Logic Gates
- Timing diagram
- Truth Table
- Gate Delay

LogicWorks

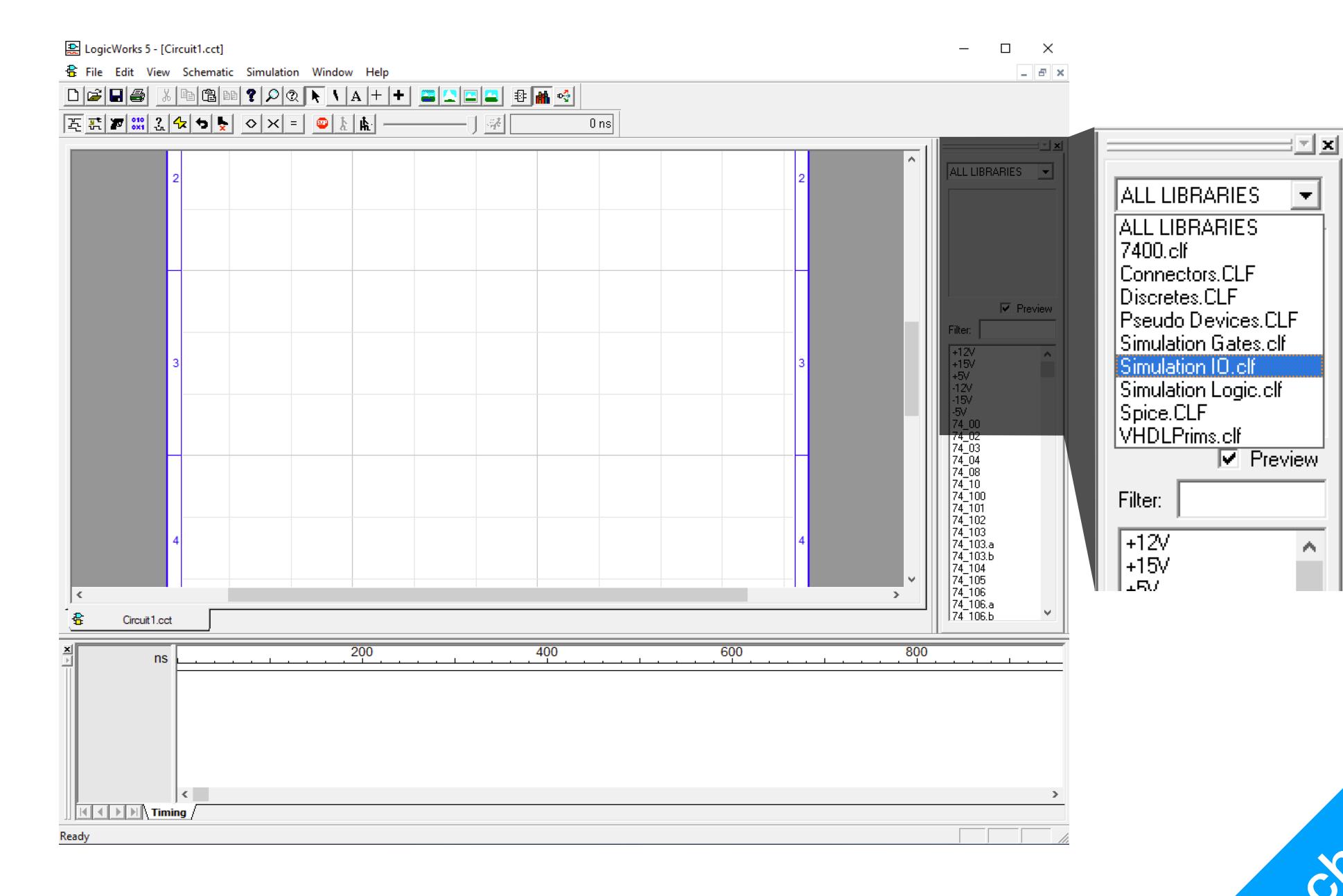
Fire up your computer please!



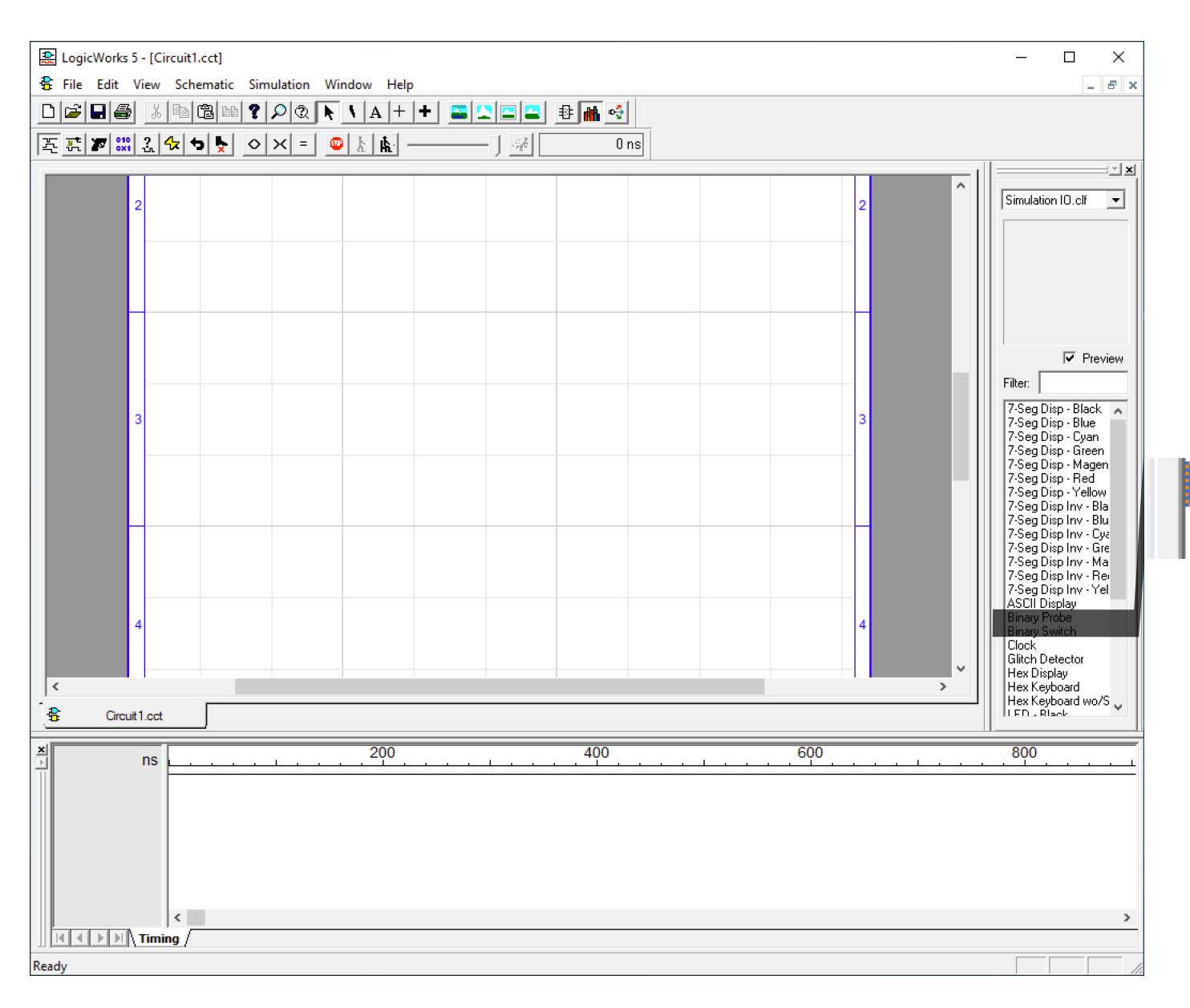
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1. This is the main interface

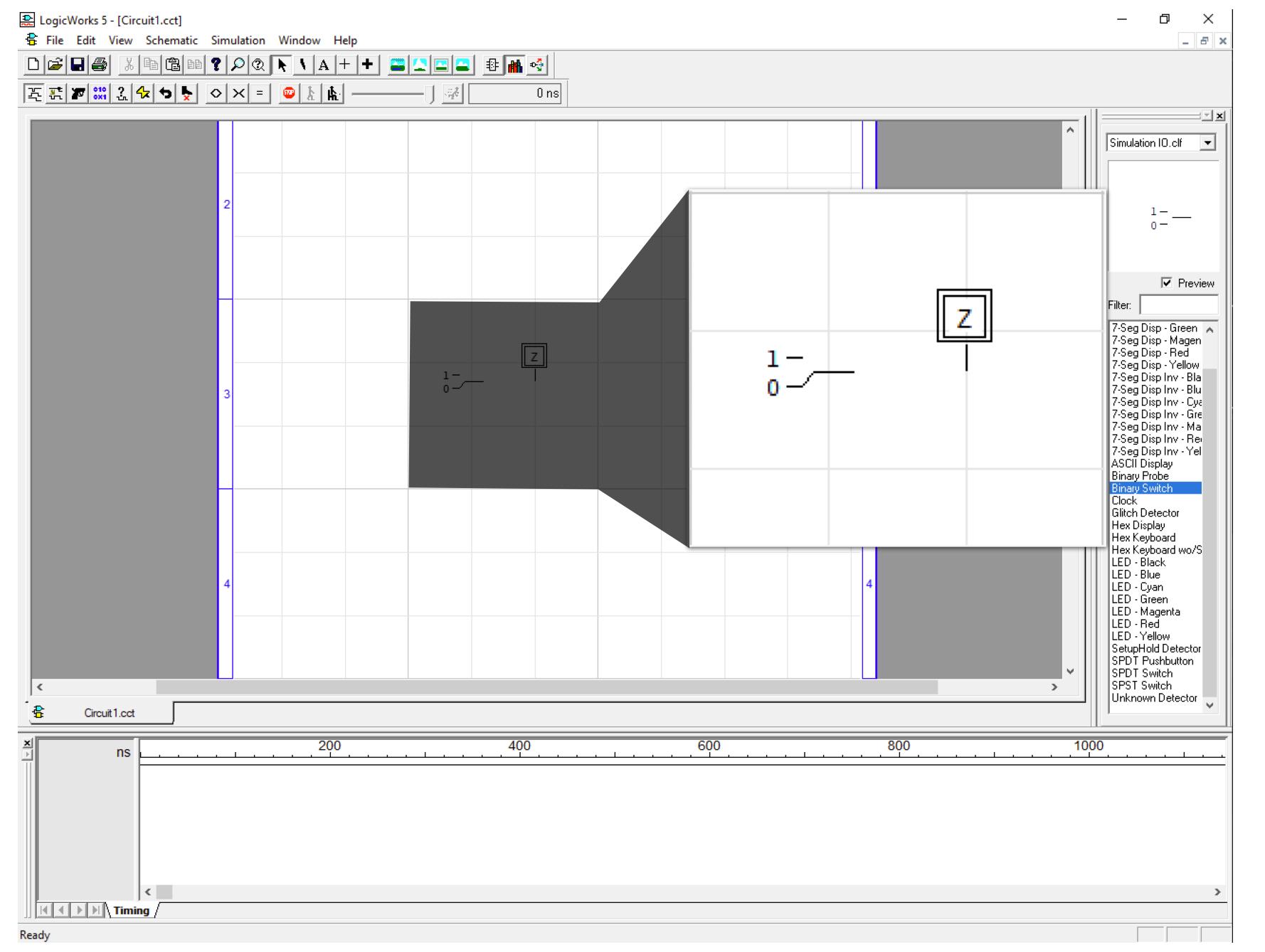


1. Select Simulation IO from the Parts Palette

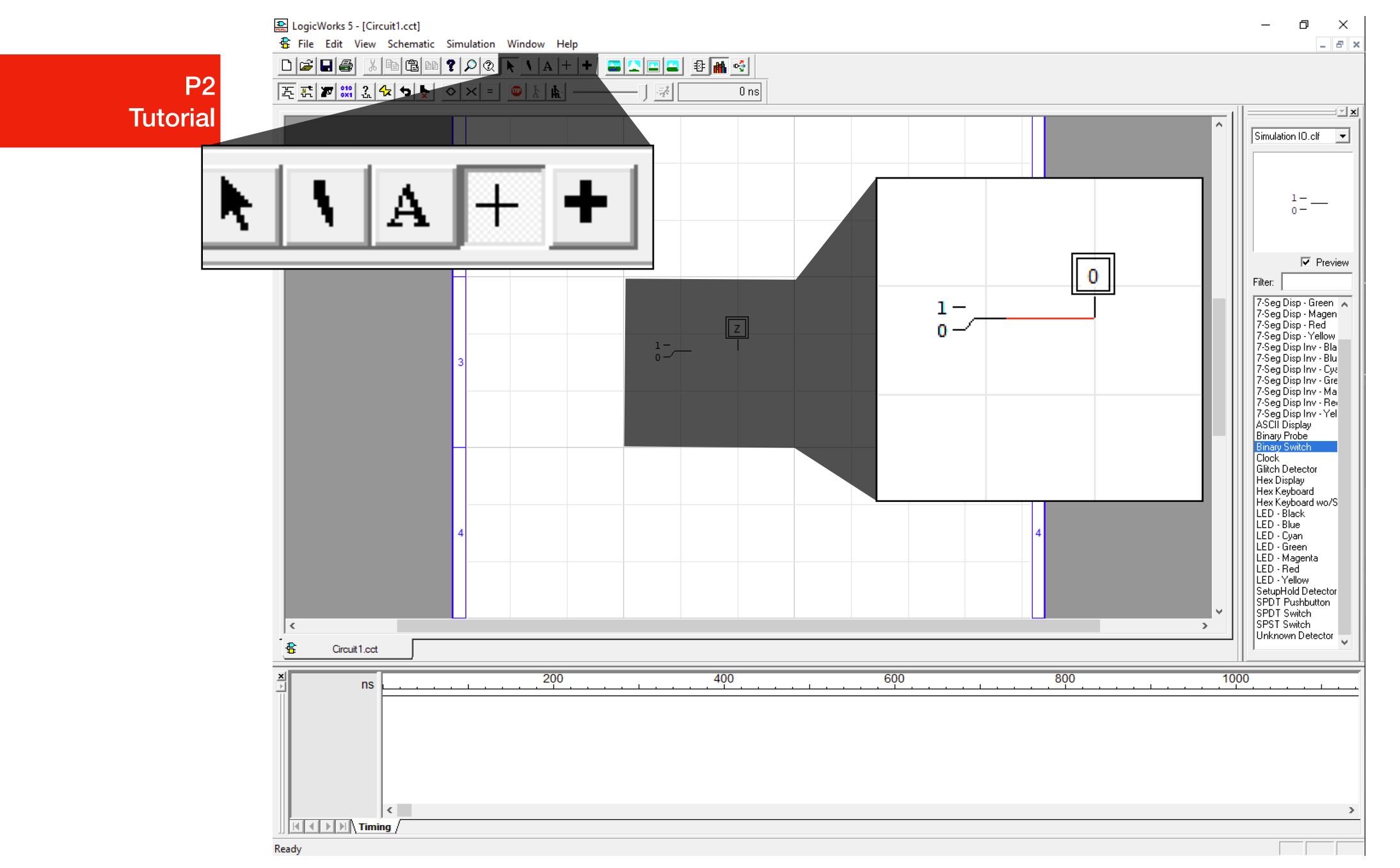


Binary Probe Binary Switch

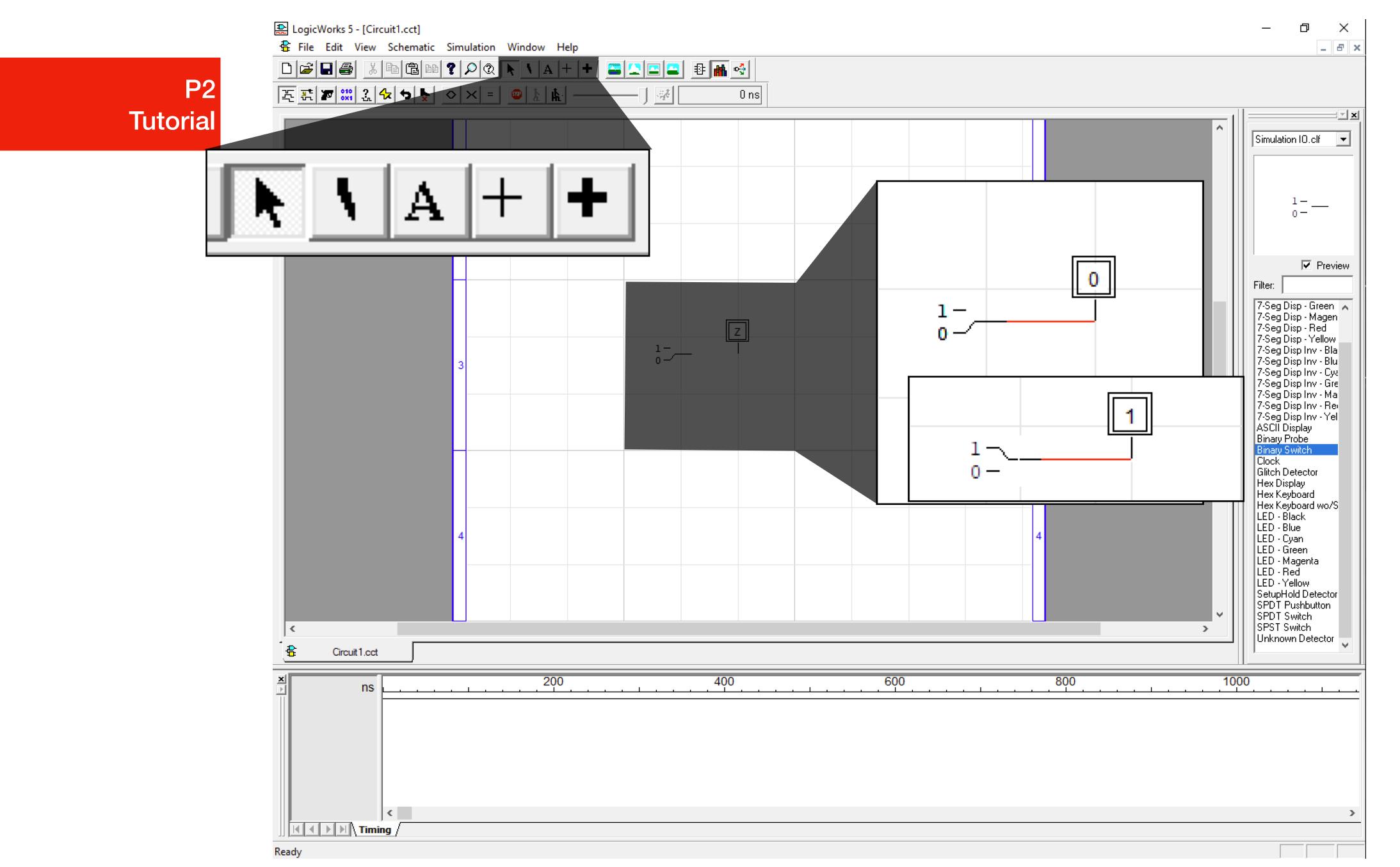
1. Pay Attention to Binary Probe and Binary Switch



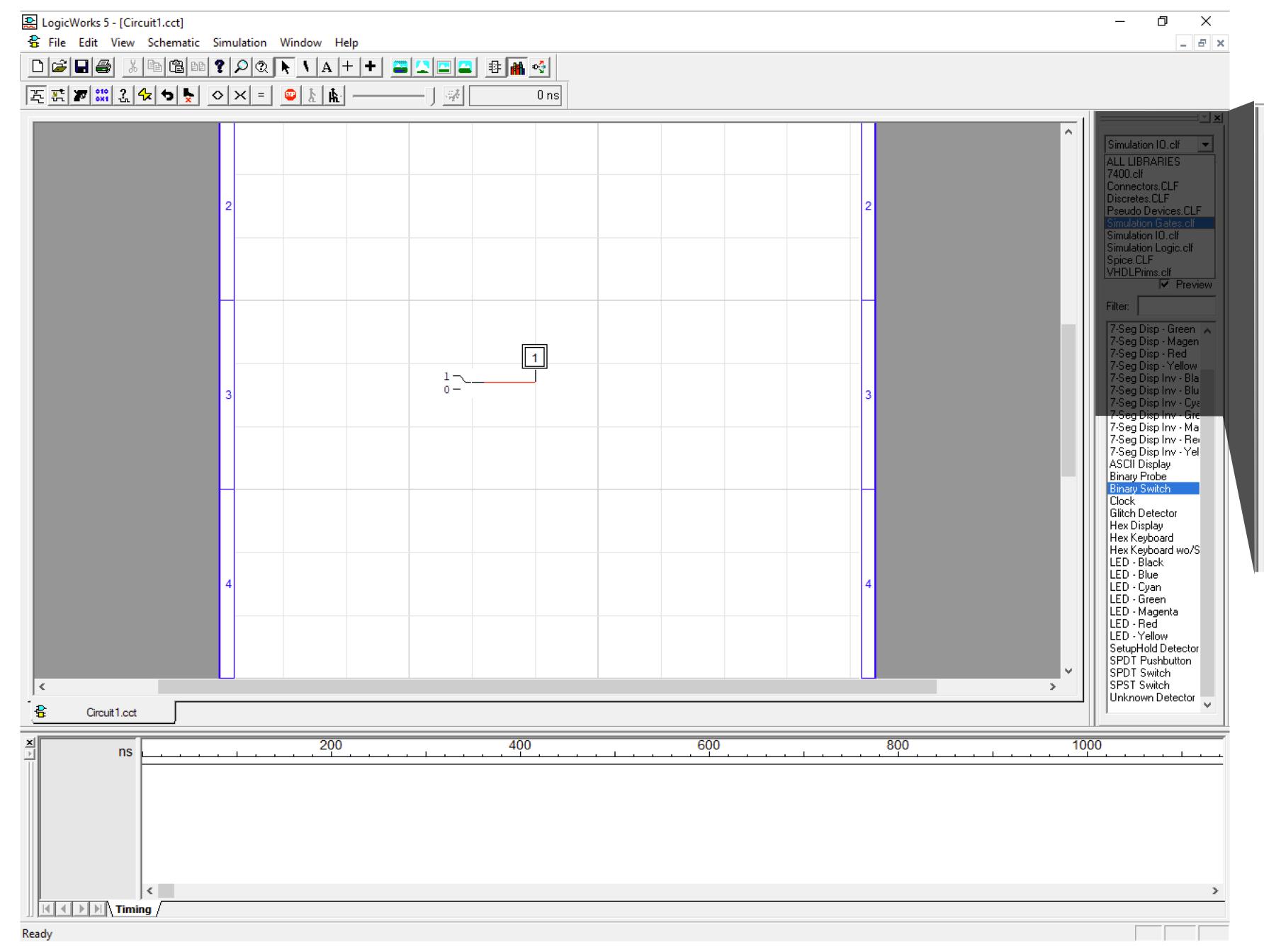
1. Double click and place one of each on the main board



1. Use the 'Draw Signal' tool to connect the two parts



1. Switch back to the Cursor mode, now click on the switch and you can change the signal value



Simulation IO.clf

ALL LIBRARIES

Connectors.CLF

Pseudo Devices.CLF

Simulation Gates.clf

Simulation Logic.clf

7-Seg Disp - Green 🔥 7-Seg Disp - Magen 7-Seg Disp - Red

✓ Preview

Simulation IO.clf

VHDLPrims.clf

Spice.CLF

Filter:

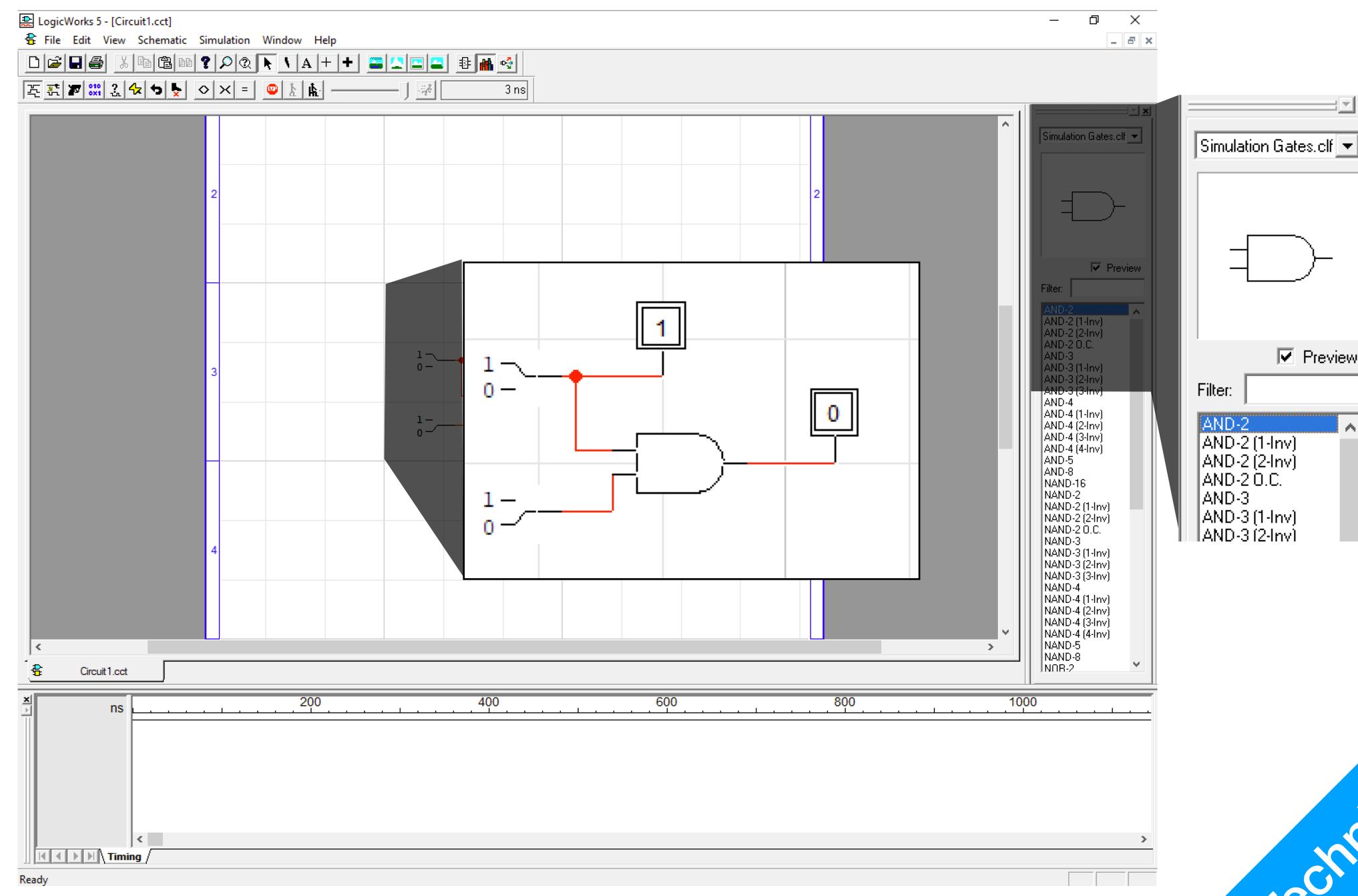
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1. Select Simulation Gates

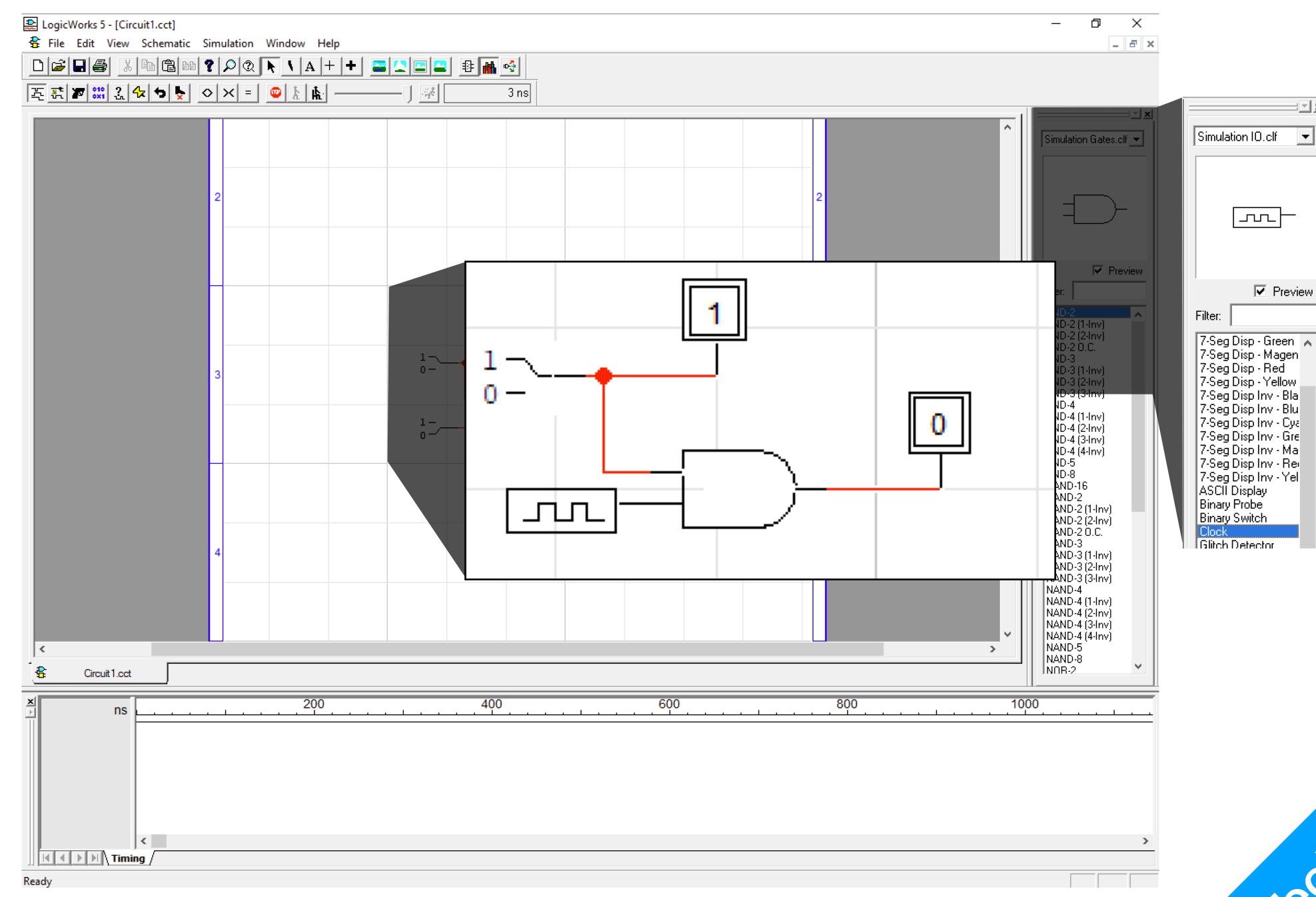
Tutorial



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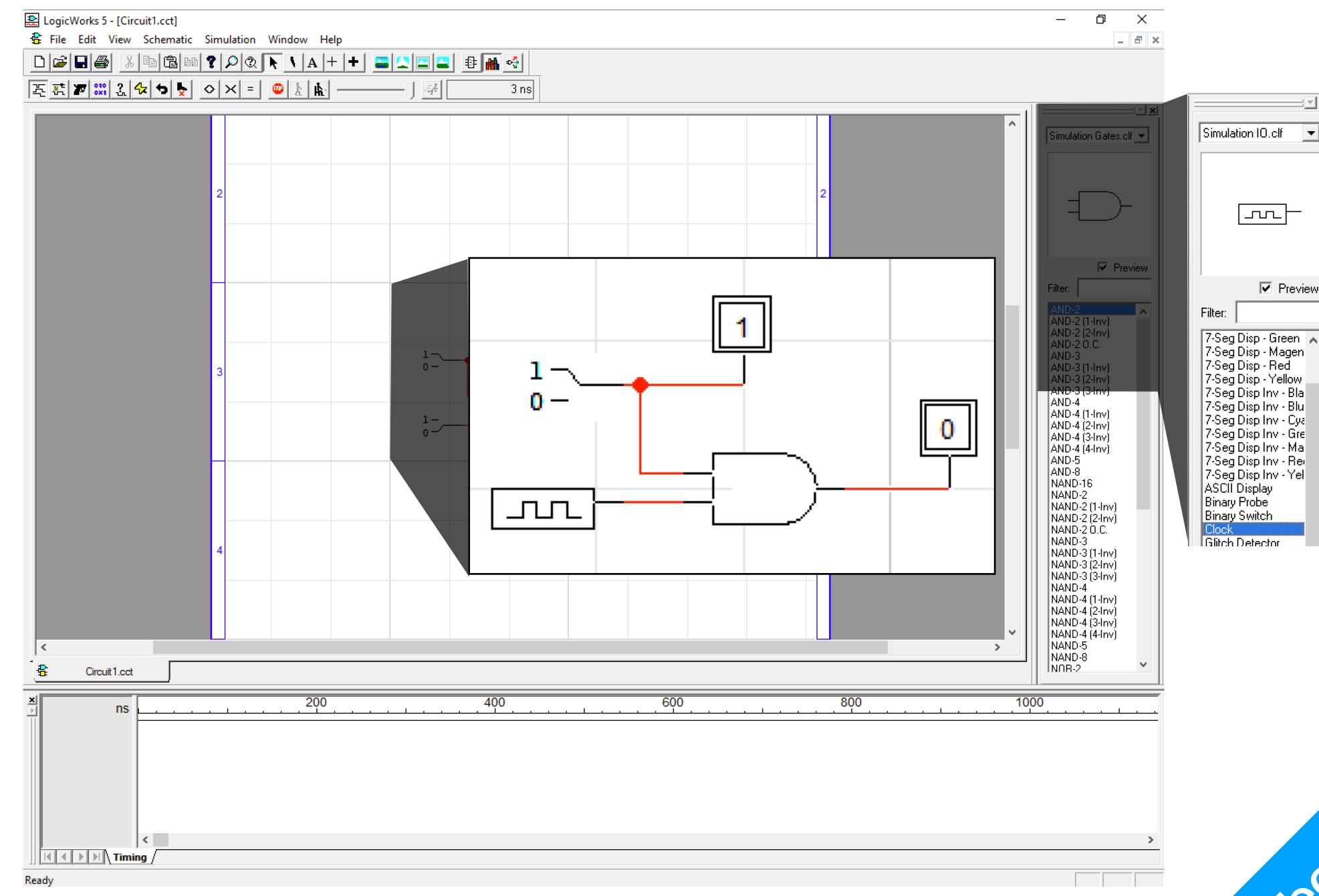
✓ Preview

1. Select AND-2, then complete the above diagram



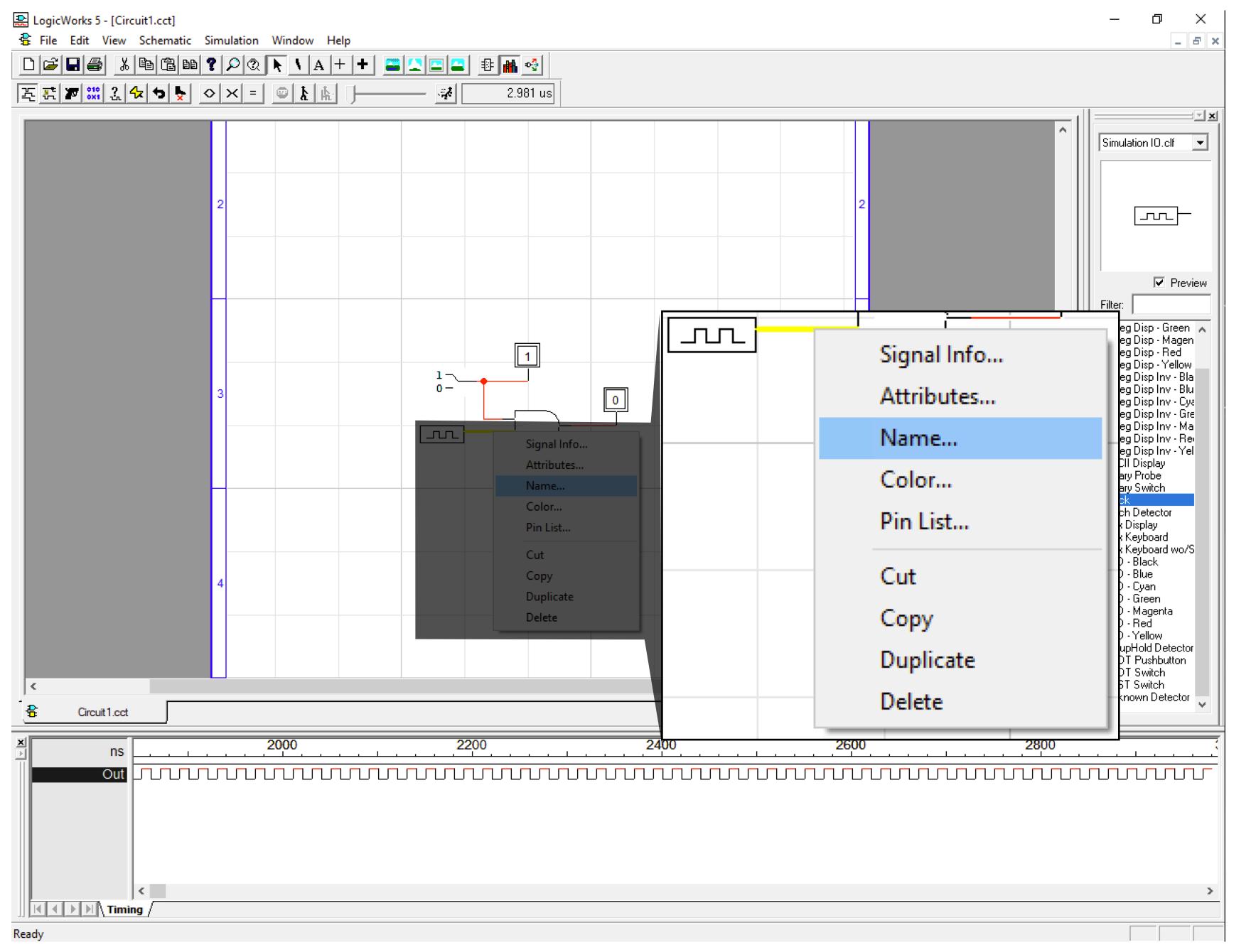
1. Select Clock from Simulation IO, then replace the lower Binary Switch with it. A Clock is a device that generates a 1 at a certain frequency

Tutorial



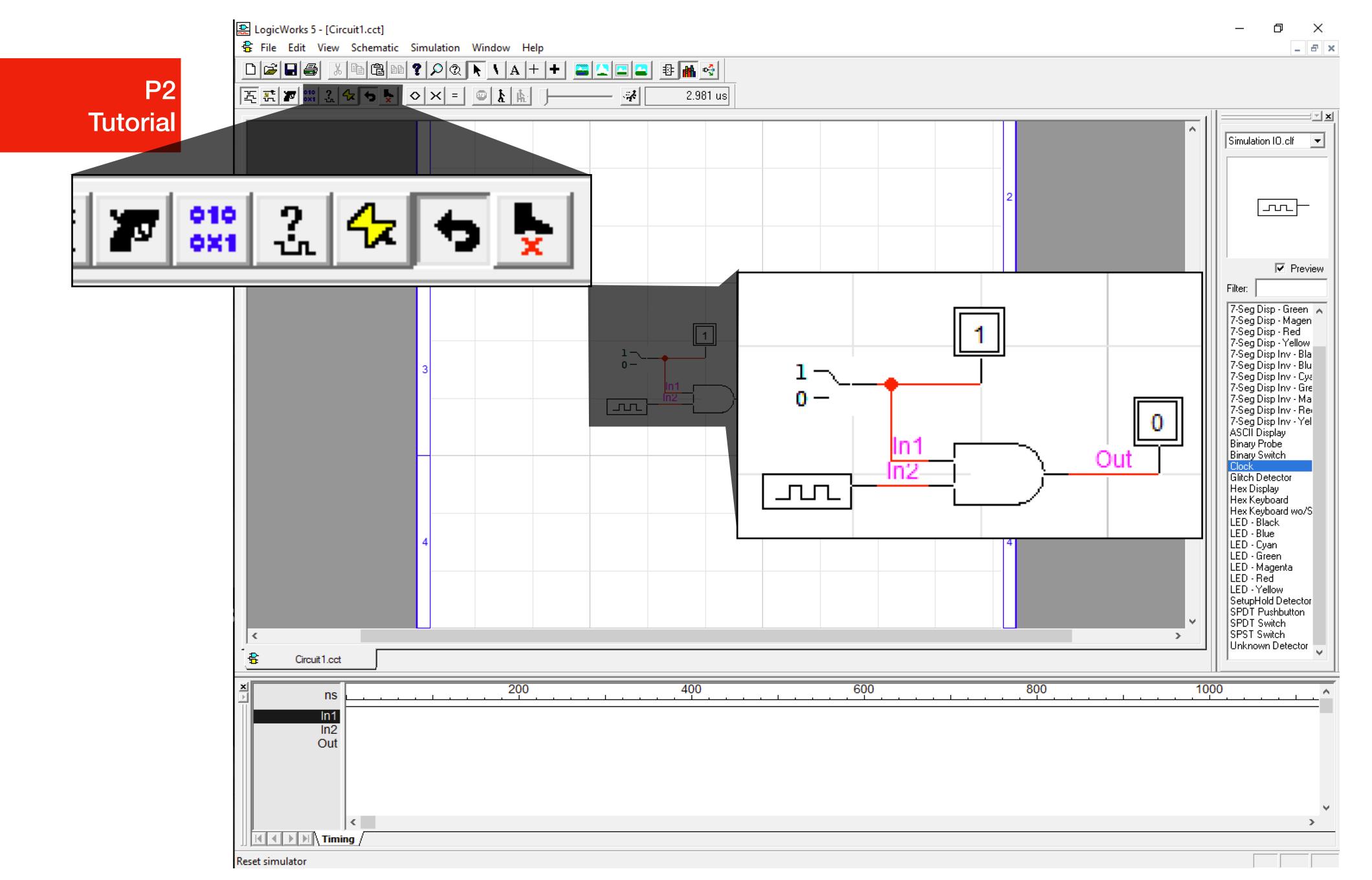
▼ Preview

1. Select Clock from Simulation IO, then replace the lower Binary Switch with it



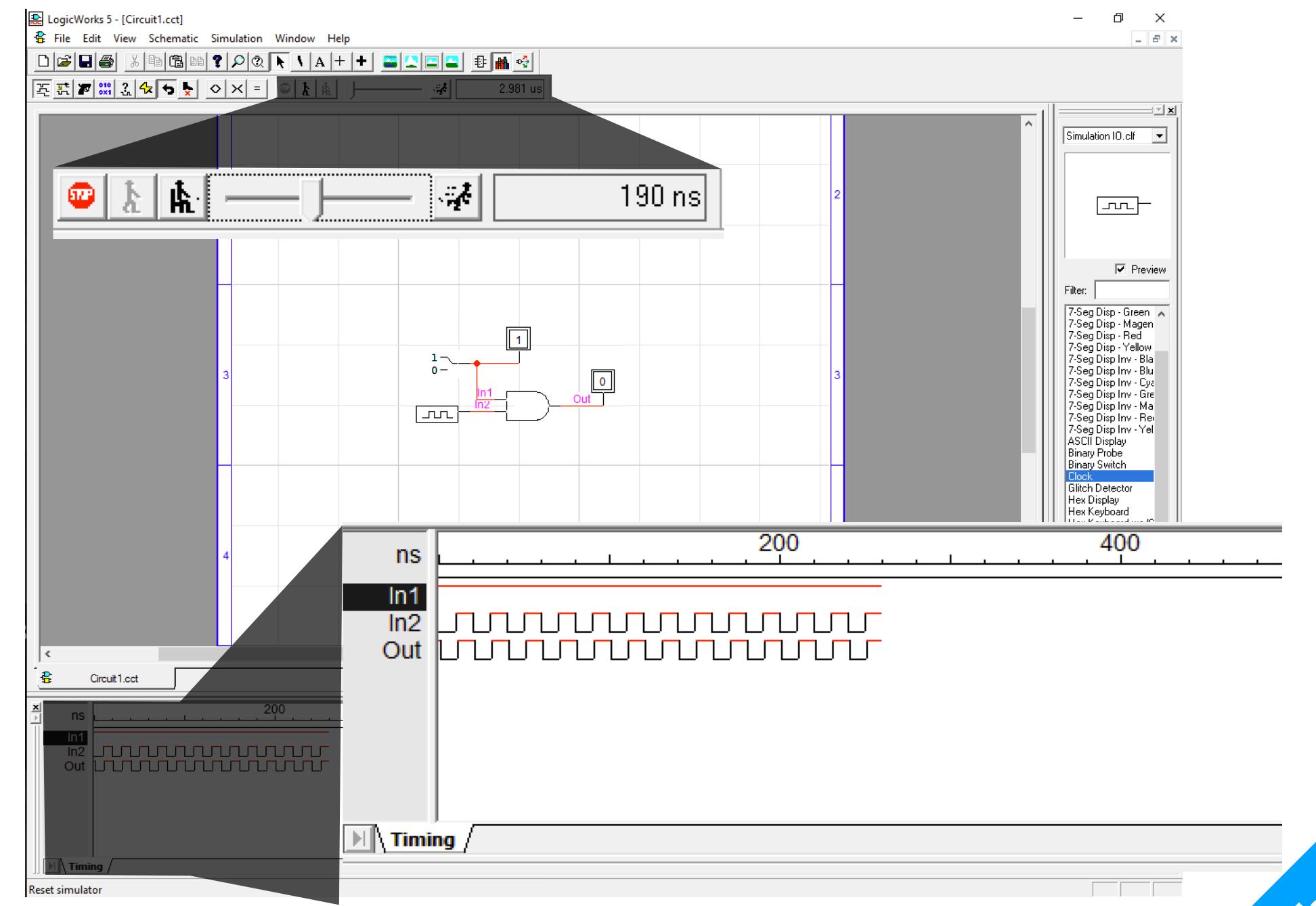
1. Right click the Red Wire, select Name

Yeculiic.



1. Complete the diagram like above, then click Reset Simulation

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1. Use the Simulation Panel to control the speed of simulation, then you will see the Timing Diagram!

Exe 1

- Curtain Motor Control
 - Button1: 1 when user wants to open the curtain
 - Button2: 1 when user wants to close the curtain
 - Output1: 1 to make the motor open the curtain
 - Output2: 1 to make the motor close the curtain
 - Light: motor is active



 When both buttons are pressed, motors do nothing

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Exe 2

- Curtain Motor Control
 - Sensor1: 1 when curtain is fully closed
 - Sensor2: 1 when curtain is fully open
 - Button1: 1 when user wants to open the curtain
 - Button2: 1 when user wants to close the curtain
 - Output1: 1 to make the motor open the curtain
 - Output2: 1 to make the motor close the curtain
 - Light: motor is active



 Stop the motor when the curtain is already fully opened/ closed

Summary

- Simulation in LogicWorks
- Binary Probe / Binary Switch in LogicWorks
- Gates in LogicWorks
- Clocks in LogicWorks
- Timing Diagram in LogicWorks