### CSCI 150 Introduction to Digital and Computer System Design Lecture 6: Memory I



Jetic Gū 2020 Summer Semester (S2)



### Overview

- Focus: Fundamentals of Complex Digital Circuit Design
- Architecture: von Neumann
- Textbook v4: Ch8 8.1, 8.2, 8.3; v5: Ch7 7.1, 7.2, 7.3
- Core Ideas:
  - 1. Memory Definition
  - 2. Read Only Memory
  - 3. Random Access Memory



















### Memory Definition Wait... do I have to remember that?



## Memory Definition

- A collection of cells capable of storing binary information
- providing temporary or permanent storage for substantial amounts of binary information
  - Substantial: much much much more than registers in a CPU
  - Temporary: e.g. DDR4 memory sticks
  - Permanent: e.g. IO devices (SSD, HDD), ROM





### **Computers In Theory**

Input/Output devices





## **Computers In Reality**

- IO data is passed to the memory before being processed
- IO data is passed from the memory after being processed





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Input/Output devices

Raw Data



## **Computers In Reality**

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Input/Output devices

Proc. Data



## 2 Types of Memories

• RAM (Random Access Memory) Memory Read Operation: retrieves information from memory Memory Write Operation: accepts new information for storage

**P1** 

Definition

- Volatile: require power for keeping its content
- ROM (Read Only Memory) Memory Read Operation: retrieves information from memory
  - Non-volatile: might not need constant power to keep its content
- Why do we need ROMs?





# Remember CD-ROMs?



### **The Many Types of ROMs**

- CD-ROM
- DVD-ROM
- Firmware ROM
- rewritten, and usually are non-volatile

Essentially, devices that stores information that cannot be normally erased/



**P2** ROM

- Storage:  $2^n \times m$ ,  $2^n$  words, each *m*-bits (usually m = 8, which makes a word=a byte)
  - 32-bit processor, n = 32, supports  $2^{32}$  bytes in memory ~ 4GB
- Input: address in *n*-bit binary
- Output: *m*-bits of stored information



**P2** ROM



**P2** ROM





**P2** ROM





**P2** ROM





**P2** ROM

• 8-bit processor Each address is in 8-bit, total of 256 different addresses













P2 ROM





per word?

• What is the maximum supported memory size for a CPU with 8-bit address space, 1 byte





- per word?
  - Ans:  $2^8 \times 1 = 256$

• What is the maximum supported memory size for a CPU with 8-bit address space, 1 byte





- per word?
  - Ans:  $2^8 \times 1 = 256$
- per word?

### • What is the maximum supported memory size for a CPU with 8-bit address space, 1 byte

### • What is the maximum supported memory size for a CPU with 16-bit address space, 1 byte





- per word?
  - Ans:  $2^8 \times 1 = 256$
- per word?
  - Ans:  $2^{16} \times 1 = 65536$

### • What is the maximum supported memory size for a CPU with 8-bit address space, 1 byte

### • What is the maximum supported memory size for a CPU with 16-bit address space, 1 byte





- What is the maximum supported memory per word?
  - Ans:  $2^8 \times 1 = 256$
- What is the maximum supported memory per word?
  - Ans:  $2^{16} \times 1 = 65536$
- What is the maximum supported memory per word?

### • What is the maximum supported memory size for a CPU with 8-bit address space, 1 byte

#### • What is the maximum supported memory size for a CPU with 16-bit address space, 1 byte

#### • What is the maximum supported memory size for a CPU with 16-bit address space, 2 bytes





- What is the maximum supported memory per word?
  - Ans:  $2^8 \times 1 = 256$
- What is the maximum supported memory per word?
  - Ans:  $2^{16} \times 1 = 65536$
- What is the maximum supported memory per word?
  - Ans:  $2^{16} \times 2 = 131072$

### • What is the maximum supported memory size for a CPU with 8-bit address space, 1 byte

#### • What is the maximum supported memory size for a CPU with 16-bit address space, 1 byte

#### • What is the maximum supported memory size for a CPU with 16-bit address space, 2 bytes



P2 ROM

![](_page_33_Picture_2.jpeg)

![](_page_34_Picture_1.jpeg)

### • 64-bit CPUs have 64-bit memory space, each word 8-bits

![](_page_34_Figure_4.jpeg)

![](_page_35_Picture_1.jpeg)

- 64-bit CPUs have 64-bit memory space, each word 8-bits
- What is the maximum supported memory size for a 64-bit CPU?

![](_page_35_Figure_6.jpeg)

![](_page_36_Picture_1.jpeg)

- 64-bit CPUs have 64-bit memory space, each word 8-bits
- What is the maximum supported memory size for a 64-bit CPU?
  - Ans: 2<sup>64</sup> × 1 = 18,446,744,073,709,551,616 = 17 million Terabytes (16 exabytes)

![](_page_36_Figure_5.jpeg)

![](_page_37_Picture_0.jpeg)

![](_page_37_Picture_1.jpeg)

#### *n*-bit address input

### **ROM Abstraction**

 $2^n \times m \text{ ROM}$ 

![](_page_37_Figure_6.jpeg)

5-bit address input

![](_page_38_Figure_2.jpeg)

 $2^5 \times 8 \text{ ROM}$ 

![](_page_38_Figure_5.jpeg)

### Rom Rom Implementation Example

5-bit address input

![](_page_39_Figure_2.jpeg)

 $2^5 \times 8 \text{ ROM}$ 

![](_page_39_Figure_5.jpeg)

5-bit address input

![](_page_40_Figure_2.jpeg)

 $2^5 \times 8 \text{ ROM}$ 

![](_page_40_Figure_6.jpeg)

5-bit address input

![](_page_41_Figure_2.jpeg)

 $2^5 \times 8 \text{ ROM}$ 

→ 8-bit data output

 This ROM has value 10010011 at address 01h;

![](_page_41_Figure_6.jpeg)

5-bit address input

![](_page_42_Figure_2.jpeg)

![](_page_42_Figure_3.jpeg)

#### → 8-bit data output

 This ROM has value 10010011 at address 01h; value 10100100 at address 1Ch;

![](_page_42_Picture_6.jpeg)

5-bit address input

![](_page_43_Figure_2.jpeg)

![](_page_43_Figure_4.jpeg)

![](_page_43_Picture_6.jpeg)

5-bit address input

![](_page_44_Figure_2.jpeg)

![](_page_44_Figure_3.jpeg)

#### → 8-bit data output

 This ROM has value 10010011 at address 01h; value 10100100 at address 1Ch;

![](_page_44_Picture_6.jpeg)

5-bit address input

![](_page_45_Figure_2.jpeg)

![](_page_45_Figure_3.jpeg)

![](_page_45_Picture_5.jpeg)

5-bit address input

![](_page_46_Figure_2.jpeg)

![](_page_46_Figure_3.jpeg)

#### → 8-bit data output

 This ROM has value 10010011 at address 01h; value 10100100 at address 1Ch;

![](_page_46_Picture_6.jpeg)

5-bit address input

![](_page_47_Figure_2.jpeg)

![](_page_47_Figure_3.jpeg)

- This ROM has value 10010011 at address 01h;
   value 10100100 at address 1Ch;
- In reality, these wiring are done with programmable technology

![](_page_47_Picture_7.jpeg)

5-bit address input

![](_page_48_Figure_2.jpeg)

![](_page_48_Figure_3.jpeg)

- This ROM has value 10010011 at address 01h; value 10100100 at address 1Ch;
- In reality, these wiring are done with programmable technology

![](_page_48_Picture_7.jpeg)

![](_page_49_Figure_1.jpeg)

 Originally proposed as unhackable storage devices Fixed internal data, cannot be hijacked through software

![](_page_50_Figure_3.jpeg)

- Originally proposed as unhackable storage devices Fixed internal data, cannot be hijacked through software
- Usually very fast readings (not as fast as registers but usually much faster than e.g. HDD)

![](_page_51_Figure_3.jpeg)

- Originally proposed as unhackable storage devices
  Fixed internal data, cannot be hijacked through software
- Usually very fast readings (not as fast as registers but usually much faster than e.g. HDD)
- Fun fact: early SSDs were using Flash Memory technology, an Electrically Erasable ROM (like in the previous slide), which is why they were so expensive

![](_page_52_Picture_4.jpeg)

![](_page_53_Picture_0.jpeg)

## Random Access Memory

Now supporting Write in all participating memory sticks

![](_page_53_Picture_3.jpeg)

![](_page_54_Figure_0.jpeg)

#### Read/Write

Chip Select CS	Read/Write R/W	Memory Operation
0	×	None
1	0	Write to selected word
1	1	Read from selected word

![](_page_54_Figure_5.jpeg)

![](_page_55_Picture_0.jpeg)

**P3** RAM

### Steps for Write

*m*-bit data input

*n*-bit address input

**Read/Write** CS

 $2^n \times m$  RAM  $2^n$  words *m* bits per word

![](_page_55_Picture_8.jpeg)

![](_page_56_Picture_0.jpeg)

### Steps for Write

 Apply the address of the desired word to the address lines *m*-bit data input

*n*-bit address input —

Read/Write \_\_\_\_\_ CS \_\_\_\_\_  $2^n \times m$  RAM  $2^n$  words *m* bits per word

 $\downarrow$  *m*-bit data output

![](_page_56_Picture_8.jpeg)

![](_page_57_Picture_0.jpeg)

### Steps for Write

- Apply the address of the desired word to the address lines
- 2. Apply the data bits that must be stored in memory to the data input lines

*m*-bit data input

*n*-bit address input —

 $2^n \times m$  RAM  $2^n$  words *m* bits per word

![](_page_57_Picture_9.jpeg)

![](_page_58_Picture_0.jpeg)

### Steps for Write

- 1. Apply the address of the desired word to the address lines
- 2. Apply the data bits that must be stored in memory to the data input lines
- 3. Activate the Write input

*m*-bit data input

*n*-bit address input ———

Read/Write \_\_\_\_\_

 $2^n \times m$  RAM  $2^n$  words *m* bits per word

 $\downarrow$  *m*-bit data output

![](_page_58_Picture_10.jpeg)

![](_page_59_Picture_0.jpeg)

**P3** RAM

![](_page_59_Picture_2.jpeg)

*m*-bit data input

*n*-bit address input

**Read/Write** CS

 $2^n \times m$  RAM  $2^n$  words *m* bits per word

![](_page_59_Picture_8.jpeg)

![](_page_60_Picture_0.jpeg)

### 1. Apply the address of the desired word to the address lines

### Steps for Read

*m*-bit data input

*n*-bit address input

**Read/Write** CS

 $2^n \times m$  RAM  $2^n$  words *m* bits per word

![](_page_60_Picture_9.jpeg)

![](_page_61_Picture_0.jpeg)

- 1. Apply the address of the desired word to the address lines
- 2. Activate the Read input

### Steps for Read

*m*-bit data input

*n*-bit address input

**Read**/Write CS

 $2^n \times m$  RAM  $2^n$  words *m* bits per word

![](_page_61_Picture_10.jpeg)

![](_page_62_Picture_0.jpeg)

- 1. Apply the address of the desired word to the address lines
- 2. Activate the Read input

### Steps for Read

*m*-bit data input

*n*-bit address input

**Read**/Write CS

 $2^n \times m$  RAM  $2^n$  words *m* bits per word

![](_page_62_Picture_10.jpeg)

## Summary Today

- devices?
- Read Only Memory
  - And its implementation using OR gate array and decoder
- Random Access Memory
  - What does the interface look like?

Memory Definition: what are some memory devices? what are not memory

![](_page_63_Picture_9.jpeg)

![](_page_63_Picture_10.jpeg)