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CSCI 150
Introduction to Digital and Computer System Design
Lecture 3: Combinational Logic Design V

Jetic Gū

2020 Summer Semester (S2)

Overview

- Focus: Arithmetic Functional Blocks
- Architecture: Combinatory Logical Circuits
- Textbook v4: Ch4 4.2; v5: Ch3 3.9
- Core Ideas:
    1. Binary Adder

P0
Review

Systematic Design Procedures

1. **Specification**: Write a specification for the circuit

2. **Formulation**: Derive relationship between inputs and outputs of the system e.g. using truth table or Boolean expressions

3. **Optimisation**: Apply optimisation, minimise the number of logic gates and literals required

4. **Technology Mapping**: Transform design to new diagram using available implementation technology

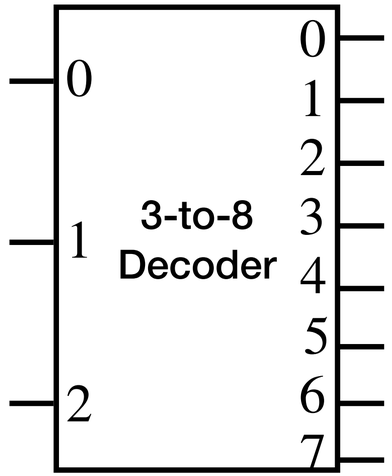
5. **Verification**: Verify the correctness of the final design in meeting the specifications

Review

P0
Review

Functional Components (1)

- Value-Fixing, Transferring, Inverting, Enabler
- Decoder
  - Input: $A_0 A_1 \ldots A_{n-1}$
  - Output: $D_0 D_1 \ldots D_{2^n-1}$, $D_i = m_i$

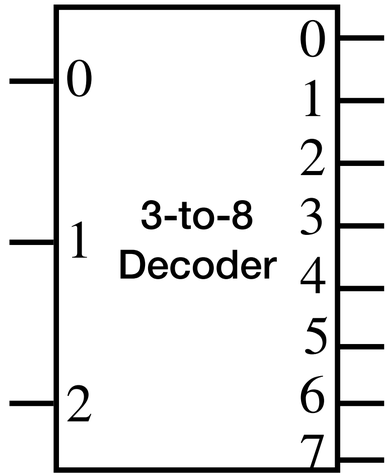


Review

P0
Review

Functional Components (2)

- Encoder
  - Input: $m_0, \ldots, m_{2^n-1}$ with only one positive value
  - Output: $A_0, \ldots, A_{n-1}$
  - Priority Encoder: validity, priority output
- Multiplexer
  - Switching between multiple input channels



Review

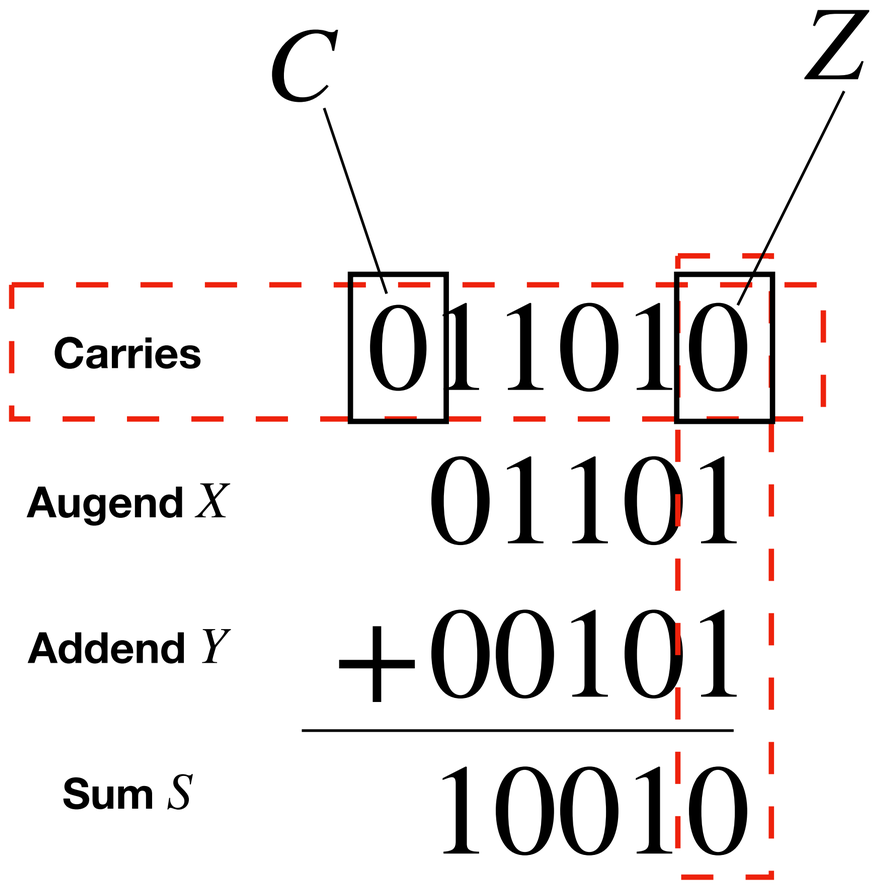
Binary Adder

The good stuff begins

Summary

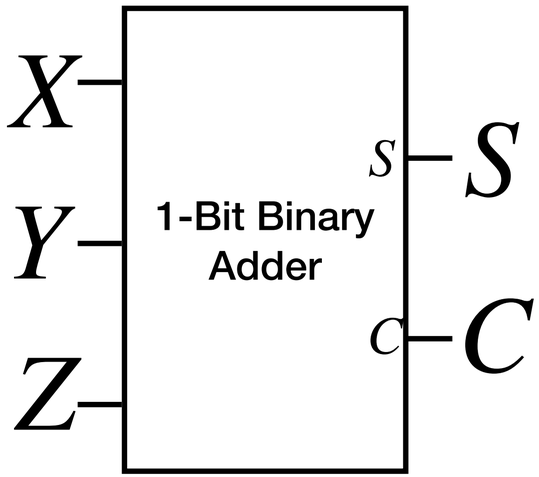
Binary Adder

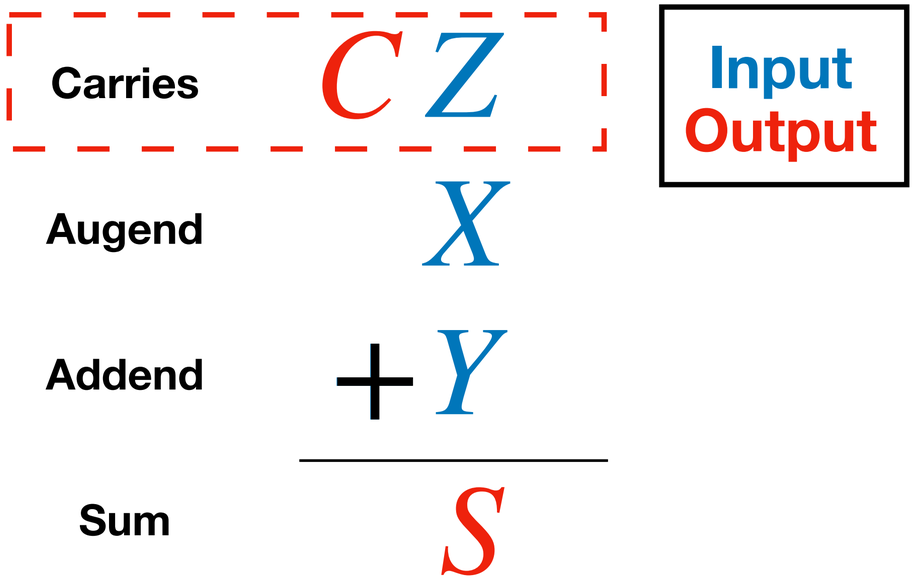
- Perform binary addition
- 1-bit Half adder
  input X, Y;
  output S, C
- Full adder
  input vectors X, Y, and single-bit Z;
  output vector S and single-bit C
- Remember what we did before?



Concept

1-bit Binary Adder



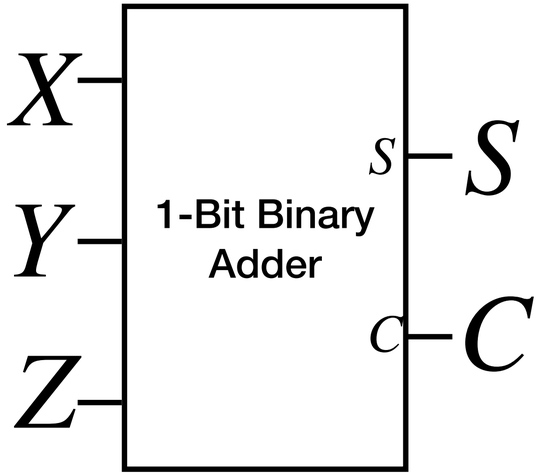


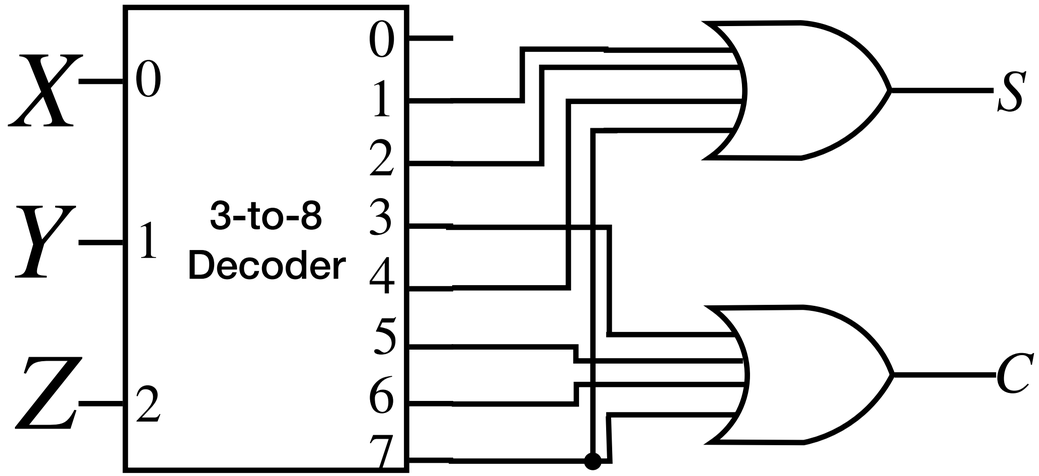
Full Adder

Review

1. #04-2020-1000-111_Lecture3_Combinational_Logic_Design_III, P3

1-bit Binary Adder





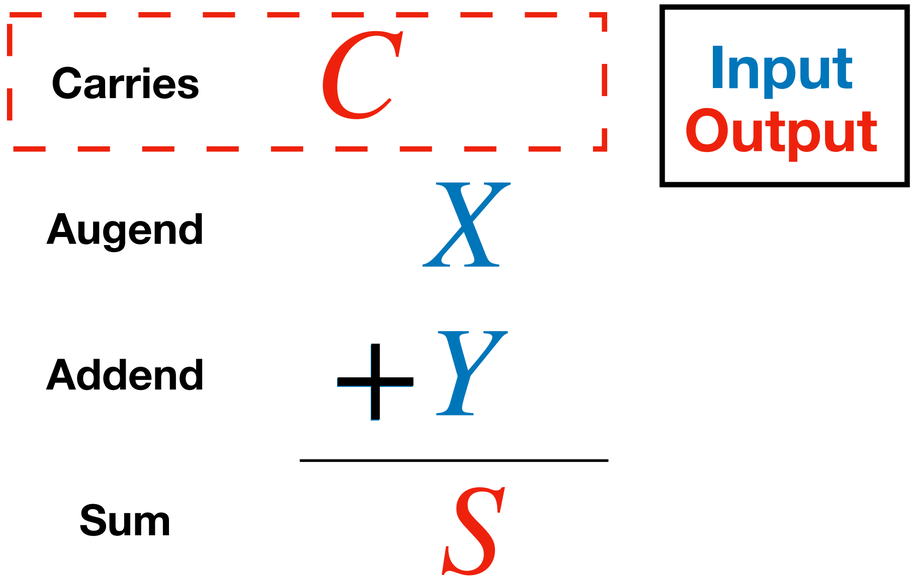
Full Adder

Review

1. #04-2020-1000-111_Lecture3_Combinational_Logic_Design_III, P3

1-bit Half Adder

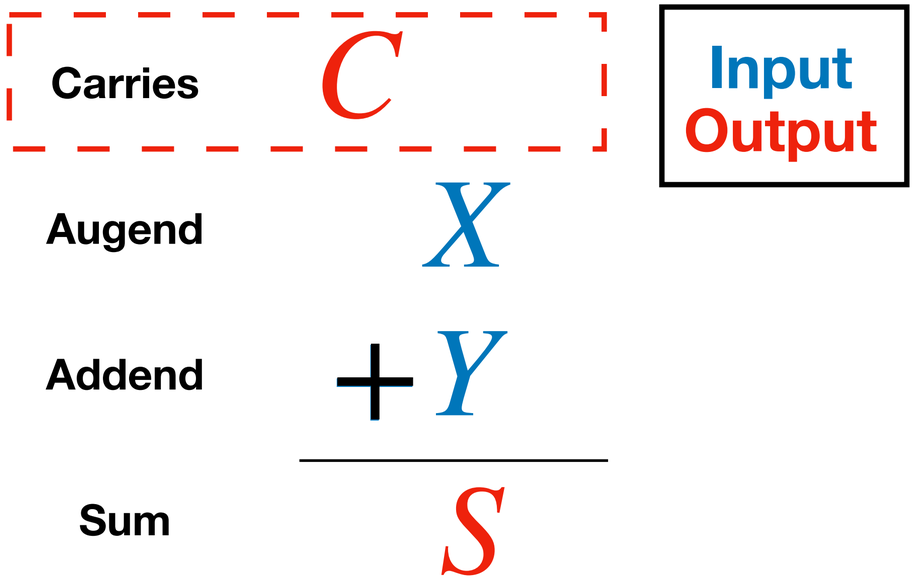
- Half adder
  input X, Y
  output S, C



Concept

P1
Binary Adder

1-bit Half Adder



Input
Output

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Concept

1-bit Half Adder

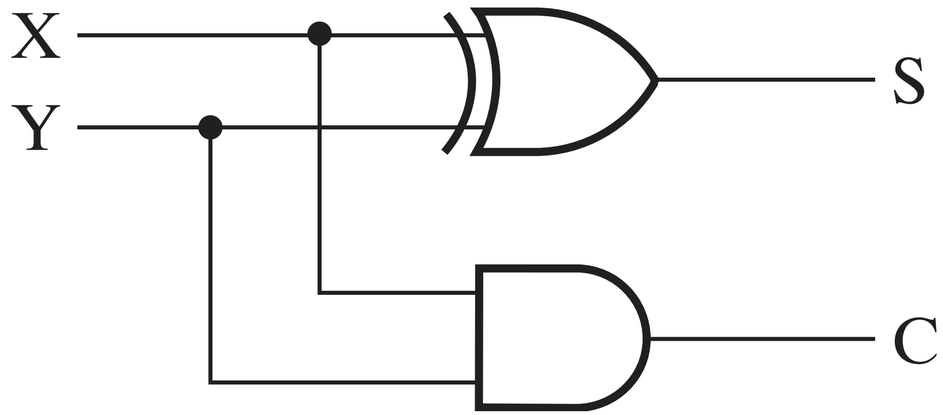
Carries C

Augend X

Addend $+Y$

Sum S

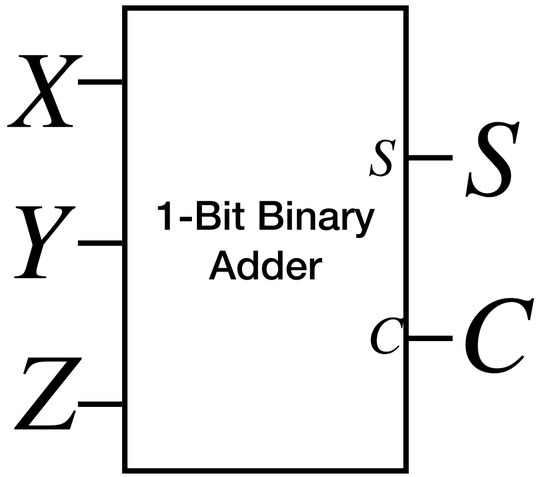
Input
Output

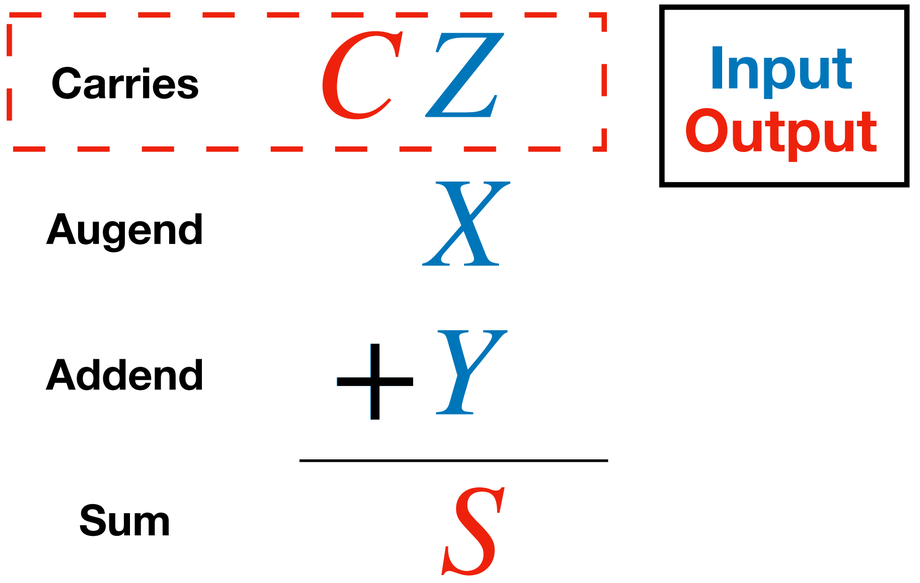


Concept

1-bit Full Adder

- Full adder input X, Y, Z; output S, C





Concept

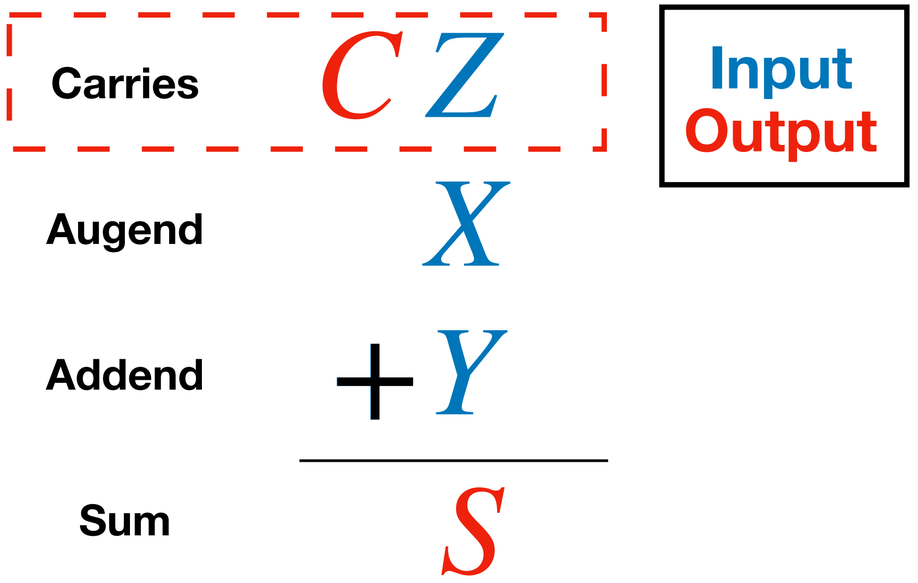
1-bit Full Adder

- Full adder
  input X, Y, Z;
  output S, C

- Half adder1
  input X, Y
  output S', C'

- Half adder2
  input S', Z
  output S, C''

$$C = C' + C''$$



Concept

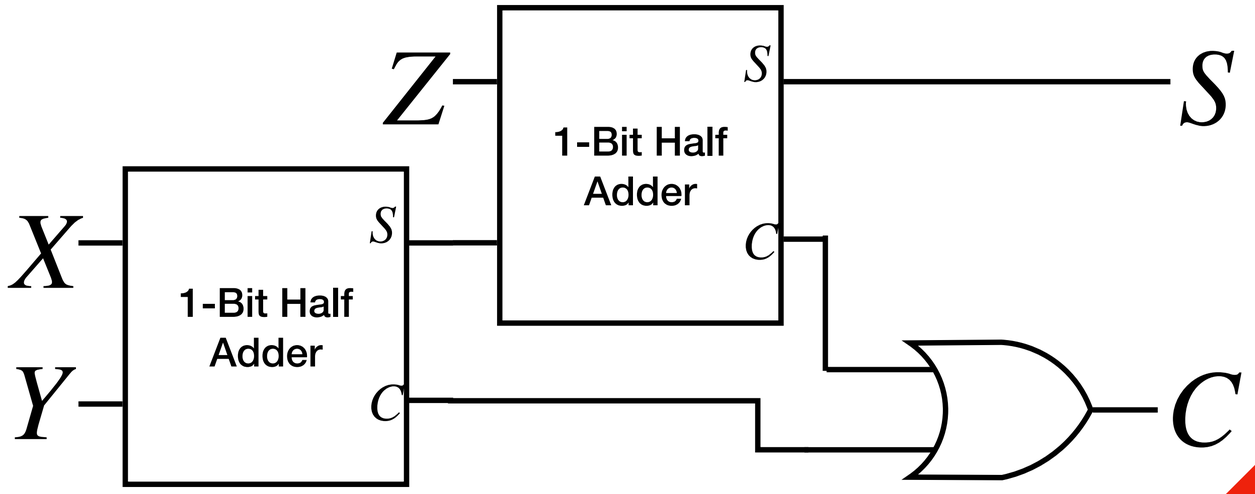
1-bit Full Adder

- Full adder
  input X, Y, Z;
  output S, C

- Half adder1
  input X, Y
  output S', C'

- Half adder2
  input S', Z
  output S, C''

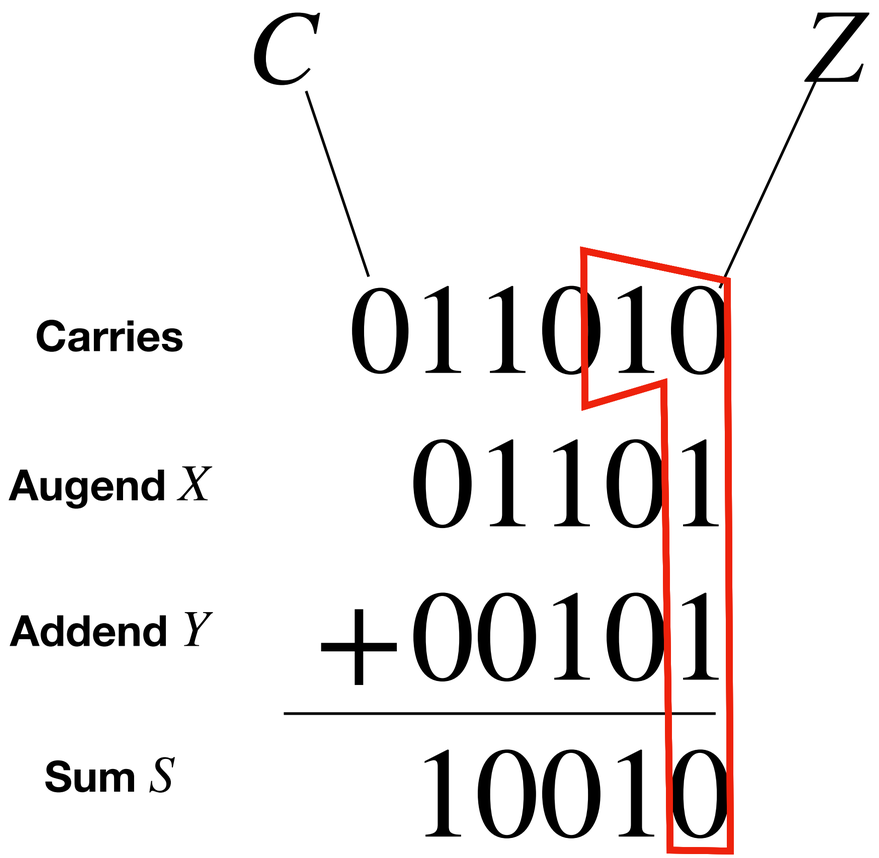
$$C = C' + C''$$



Concept

n-bit Full Adder

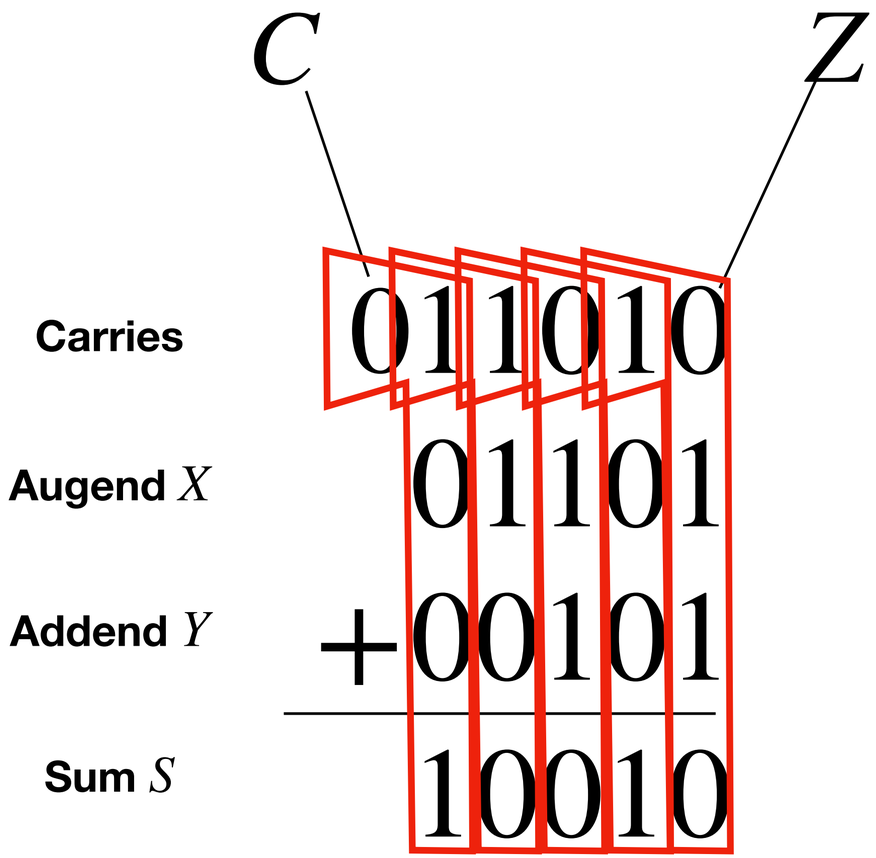
- Full adder
  input vectors X, Y, and single-bit Z;
  output vector S and single-bit C



Concept

n-bit Full Adder

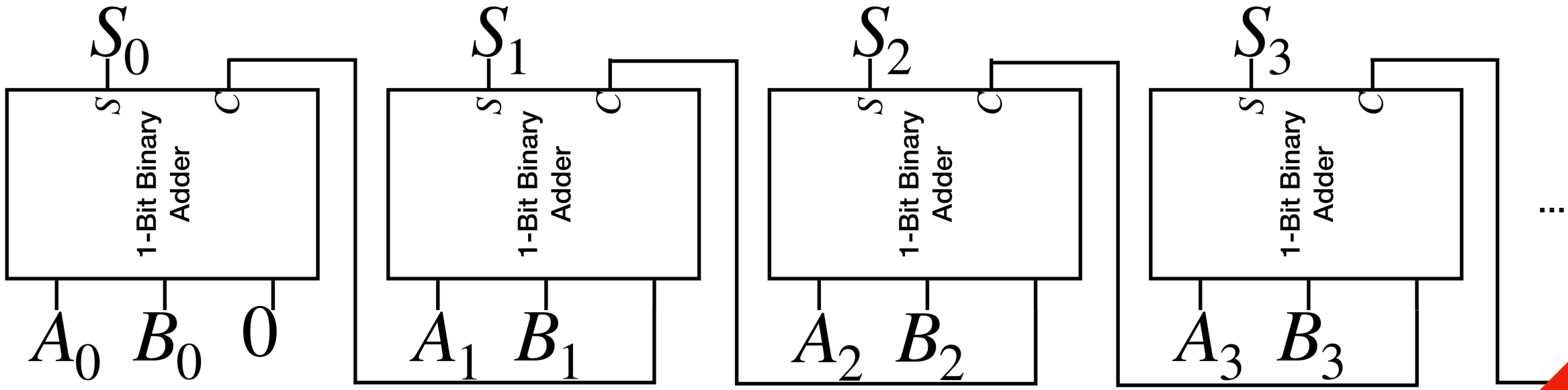
- Full adder
  input vectors X, Y, and single-bit Z;
  output vector S and single-bit C



Concept

n-bit Full Adder

- Ripple Carry Adder



Concept

PX
Future

Preview

- Binary Adder √
- Binary Subtraction (using complements)
- Adder-Subtractor Unit
- Contraction, Incrementing, Multiplication (by constant), Division (by constant)
- VHDL

Future