Name		Quiz Date	2020.02.31
Student #		Time	180min
Mark		Full Mark	30pt

08.04.20 09:16

Please remember to write your name and student number. Calculators are not allowed. The consequences of cheating will be severe (death by Tiger).

Final Exam

1. (5pt) Multiple choice questions

I. Which of the following is not a major component in von Neumann architecture?

A. I/O devices

B. Central Processing Unit

C. Datapath

D. Memory

II. Which of the following components may be used to select a register from a register array?

A. Decoder

B. Enabler

C. Encoder

D. Multiplexer

III. What is the advantage of synchronous counter over ripple counter?

A. Less propagation delay

B. More correct

C. Less number of flip-flops

D. None of above

IV. Which of the following are acceptable state assignments for a finite-state machine with 3 states (X, Y, Z)?

A. $X = 0001, Y = 0101, Z = 1000$

B. $X = 001, Y = 010, Z = 100$

C. $X = 00\text{X}, Y = 01\text{X}, Z = 1\text{XX}$

D. All of above

V. What is the purpose of parity code?

A. Data error detection

B. Data error correction

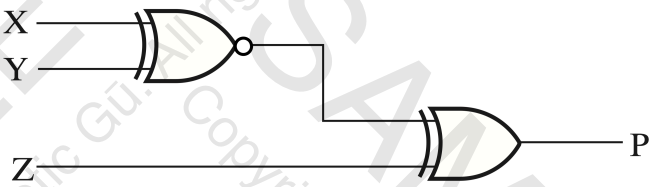
C. Hardware error detection

D. None of above

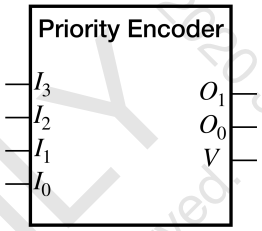
2. (5pt) Short question and answers

A. What is the signed 2s complement of signed 8-bit binary integer 10001100 and 00100110 (1pt)?

B. In the following circuit, what is the output given input $X = Y = Z = 1$ (1pt)?



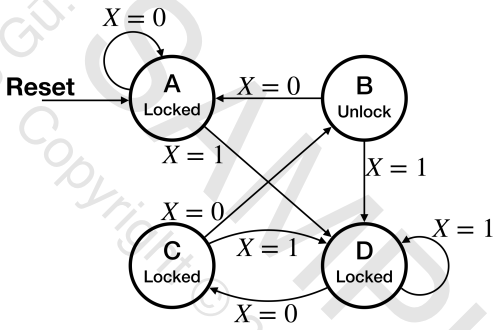
C. Given 4-to-2 priority encoder, what is the output $[O_{1:0}; V]$ given input $I_{3:0} = 0101$ (1pt)?



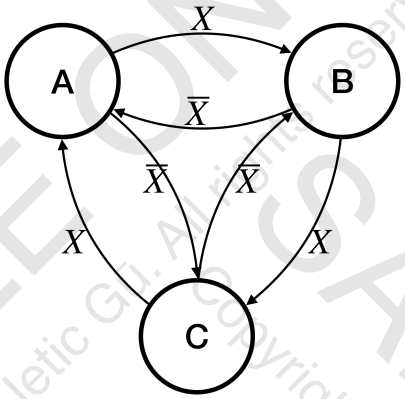
D. Write down all of the unreachable states in the following sequential circuit, given initial state 000. (Hint: draw the state table or state diagram) (1pt)

$D_A = \overline{X}\,\overline{A}\,\overline{B} + X\,\overline{A}\,B$, $D_B = \overline{B} + A\,\overline{X} + \overline{A}\,X$

E. In the following state machine diagram, the input sequence that leads to 'Unlock' is: _____ . (1pt)



3. (5pt) Sequential circuit analysis



A. Given input sequence for X being 0111011010, initial state A, what is the state transition sequence (1pt)?

B. Draw the state table by hand, include it in your submission PDF (1pt).

C. Perform one-hot state assignment, then write down the flip-flop input equations after simplification (1pt).

D. Given state assignment A=00, B=01, C=11. Write down the flip-flop input equations with unused state as don't care conditions. Optimise each flip-flop's input using K-map, and include all the steps in your submission PDF (1pt).

E. Draw the above circuit diagram by hand, include it in your submission PDF (1pt).

4. (5pt) Circuit design.

   Mr. Cheese has commissioned you to design a lock for him. The lock should only be unlocked when it receives the correct input. The lock takes 8-bit input, and the unlocking combination is 10110010. An output variable F denotes the status of the lock, $F = 1$ means it is unlocked, $F = 0$ mean it is locked.

   A. Assuming the 8-bit input is $X_{7:0}$, draw the combinational circuit diagram for the lock by hand and include it in your submission PDF. You may use any gate or functional block we've covered in class (2pt).

   B. Mr. Cheese has changed his mind and wants the input to arrive sequentially. Assuming the 1-bit input is X, and when the lock is receiving inputs it should always remain locked. When all 8-bits have arrived, the lock should depend on the combination be unlocked or remain locked. If the combination is incorrect, the lock should be ready to receive the next 8-bit input, otherwise it should remain unlocked. Draw the state machine diagram by hand and include it in your submission PDF. (It is not required to perform state assignment) (3pt)

5. (5pt) Datapath design.

   You are charged with the duty to design a datapath with eight 8-bit GPRs. The datapath has the following operations. upon receiving instruction $M_{1:0}$:

   - $M_{1:0} = 00$: Load input $X_{7:0}$ into register with address $A_{2:0}$.
   - $M_{1:0} = 01$: Output register with address $A_{2:0}$ to output $F_{7:0}$.
   - $M_{1:0} = 10$: Add register $A_{2:0}$ with input $X_{7:0}$, store the results back into register $A_{2:0}$.
   - $M_{1:0} = 11$: Swap the values of register $A_{2:0}$ and $X_{2:0}$

   Draw the circuit diagram of this datapath, with input $M_{1:0}$, $A_{2:0}$, $X_{7:0}$, output $F_{7:0}$. You may use any combinational functional blocks we've covered in class. You do not have to care about output $F_{7:0}$ in $M_{1:0} = 00,10,11$. Include the diagram in your submission PDF.

6. (5pt) Flip-Flop design

   A. Draw the diagram for a D flip-flop with D latch and SR latch. (1pt)
   B. Draw the diagram for an 4-bit register using D flip-flips. The input should be $I_{3:0}$, and there must only be one input C. (1pt)
   C. Extend the above 4-bit register with clear function. Do not modify your D flip-flop design, you must use additional gates on your design in B. (1.5pt)
   D. Extend the above design with enabler function. Do not modify your D flip-flop design, you must use additional gates on your design in C. (1.5pt)