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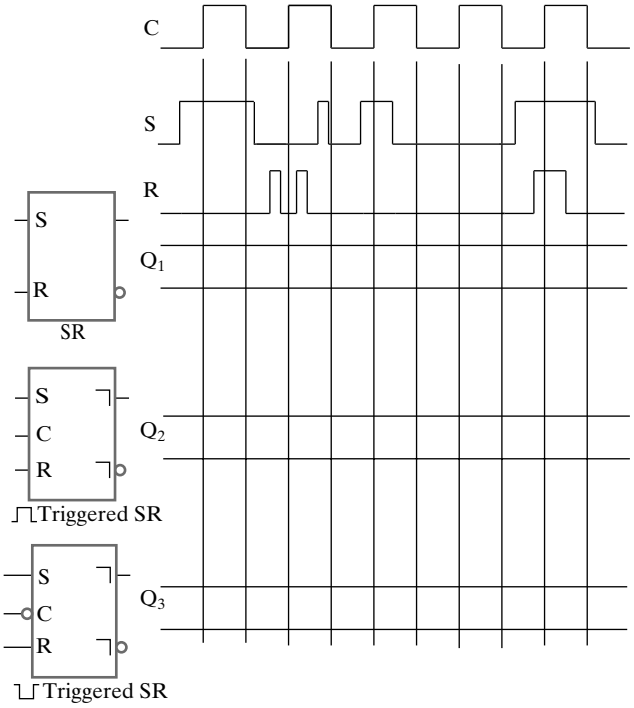
This assignment is due on 21 March. 2020

Please remember to write your name and student number.

Please submit a single PDF for each assignment. Handwritten submissions and proprietary formats (e.g. Pages or MS Word) will not be accepted. The Lab portion must be submitted separately.

Assignment 4 Answer

1. Clock, S and R waveforms, one latch and two flip-flops are shown in the following figure. For the latch and the flip-flops, carefully sketch the output waveform, Q_i, obtained in response to the input waveforms. Assume that the propagation delay of the storage elements is negligible. Initially, all storage elements store 0.



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2. A sequential circuit has three D flip-flops A, B, and C, and one input X. The circuit is described by the following input equations:

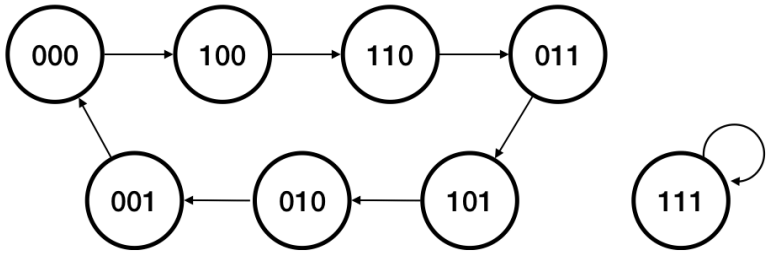
$$D_A = (B\overline{C} + \overline{B}C)X + (BC + \overline{B}\,\overline{C}\,)\overline{X}$$
$$D_B = A$$
$$D_C = B$$

   A. Derive the state table for the circuit.

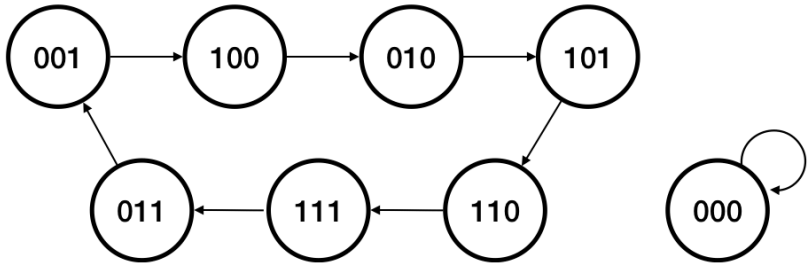
Present State			Input	Next State		
A	**B**	**C**	**X**	**A**	**B**	**C**
0	**0**	**0**	**0**	1	0	0
0	**0**	**0**	**1**	0	0	0
0	**0**	**1**	**0**	0	0	0
0	**0**	**1**	**1**	1	0	0
0	**1**	**0**	**0**	0	0	1
0	**1**	**0**	**1**	1	0	1
0	**1**	**1**	**0**	1	0	1
0	**1**	**1**	**1**	0	0	1
1	**0**	**0**	**0**	1	1	0
1	**0**	**0**	**1**	0	1	0
1	**0**	**1**	**0**	0	1	0
1	**0**	**1**	**1**	1	1	0
1	**1**	**0**	**0**	0	1	1

B. Draw two state diagrams, one for $X = 0$ and the other for $X = 1$.

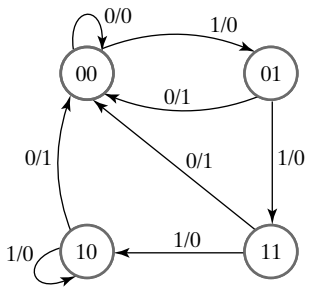
X=0



X=1



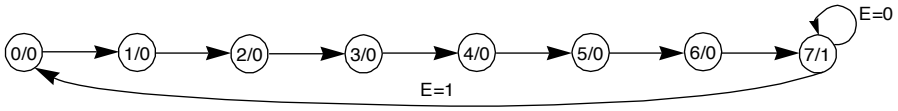
3. Starting from state 00 in the following state diagram, determine the state transitions and output sequence that will be generated when an input sequence of 10011011110 is applied.



01/0 -> 00/1 -> 00/0 -> 01/0 -> 11/0 -> 00/1 -> 01/0 -> 11/0 -> 10/0 -> 10/0 -> 00/1

4. A Universal Serial Bus (USB) communication link requires a circuit that produces the sequence 00000001. You are to design a synchronous sequential circuit that starts producing this sequence for input $E = 1$. Once the sequence starts, it completes. If $E = 1$, during the last output in the sequence, the sequence repeats. Otherwise, if $E = 0$, the output remains constant at 1.

   1. Draw the state diagram for the circuit.

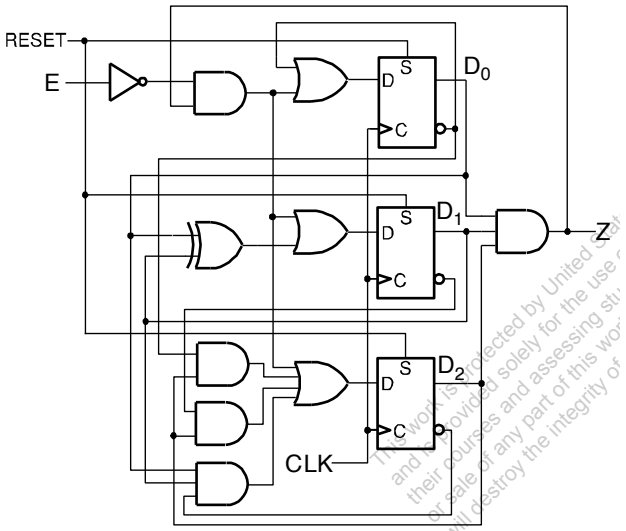


   2. Find the state table and make a state assignment.

Present state	Next State For Input		Output
$D_2D_1D_0$	E=0	E=1	Z
000	001	001	0
001	010	010	0
010	011	011	0
011	100	100	0
100	101	101	0
101	110	110	0
110	111	111	0
111	111	000	1

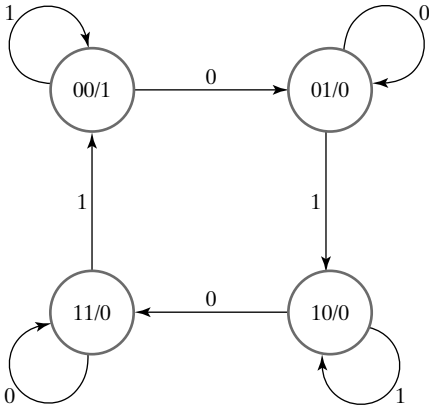
Solution not unique*

   3. Design the circuit using D flip-flops and logic gates. A reset should be included to place the circuit in the appropriate initial state at which E is examined to determine if the sequence of constant 1s is to be produced.



Solution not unique*

5. A sequential circuit has two flip-flops A and B, one input X, and one output Y. The state diagram is shown in the following figure. Design the circuit with D flip-flops using a 1-hot state assignment.



To use a one-hot assignment, the two flip-flops A and B need to be replaced with four flip-flops Y4, Y3, Y2. Y1.

No Reset State Specified.

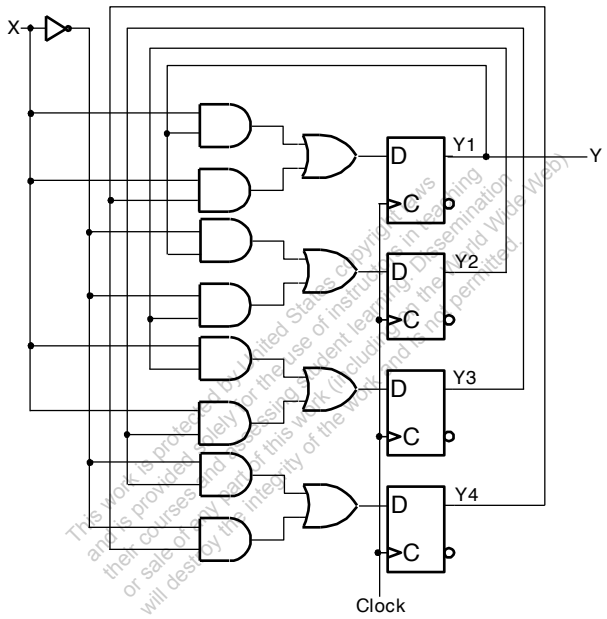
$D1 = Y1' = X \cdot Y1 + X \cdot Y4$

$D2 = Y2' = \bar{X} \cdot Y1 + \bar{X} \cdot Y2$

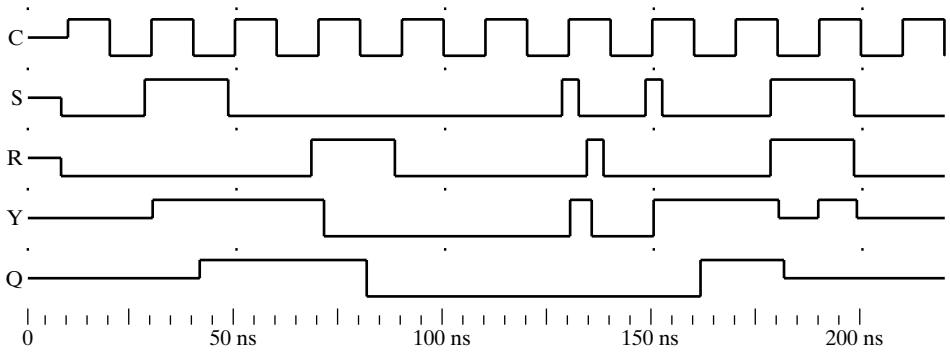
$D3 = Y3' = X \cdot Y2 + X \cdot Y3$

$D4 = Y4' = \bar{X} \cdot Y3 + \bar{X} \cdot Y4$

Present State		Input	Next State		Output
A B	*Y4 Y3 Y2 Y1*	*X*	*A' B"*	*Y4'Y3'Y2'Y1*	*Z*
0 0	0 0 0 1	0	0 1	0 0 1 0	1
0 0	0 0 0 1	1	0 0	0 0 0 1	1
0 1	0 0 1 0	0	0 1	0 0 1 0	0
0 1	0 0 1 0	1	1 0	0 1 0 0	0
1 0	0 1 0 0	0	1 1	1 0 0 0	0
1 0	0 1 0 0	1	1 0	0 1 0 0	0
1 1	1 0 0 0	0	1 1	1 0 0 0	0
1 1	1 0 0 0	1	0 0	0 0 0 1	0



6. The following figure is the logic simulation of an SR Master–Slave flip-flop. Obtain a similar timing diagram for a positive-edge-triggered JK flip-flop during four clock pulses. Show the timing signals for C, J, K, Y, and Q. Assume that initially the output Q is equal to 1, with $J = 0$ and $K = 1$ for the first pulse. Then, for successive pulses, J goes to 1, followed by K going to 0 and then J going back to 0. Assume that each input changes near the negative edge of the pulse.


C
S
R
Y
Q
0
50 ns
100 ns
150 ns
200 ns

……

Lab 3

You must complete the following assignment and submit a PDF of instructions enough to replicate your results, and required documentation. You will also need to upload LogicWork circuit design files as specified, and your own library file. Then upload a single ZIP file to student portal. If you don't have the software, draw the circuit design only and include it in the PDF.

1. Save the library and circuit files we created in class containing the following designs in the final ZIP file:

   (1) D latch (`circuit1-1.cct`);

   (2) D flip-flop (`circuit1-2.cct`);

   (3) Implement $D_A = \overline{X}A + XY$, $D_B = \overline{X}B + XA$, $Z = XB$ (`circuit1-3.cct`);

   (4) Draw the state table and diagram for (3).

2. Draw the state diagram of rotator, write down the equations for each D flip-flop, and complete the implementation (`circuit2.cct`).

   Start state $X_3X_2X_1X_0$: original 4-bit, implement using binary switches

   Input Y

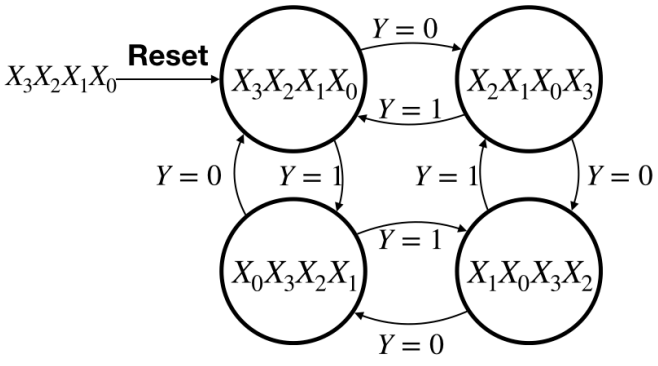
   0: for left rotation (output $X_2X_1X_0X_3$);

   1: for right rotation (output $X_0X_3X_2X_1$);

   Behaviour

   Every CLK triggers a shift

   State Diagram:



   State Assignment and Equations:

   Flip-flops A, B, C, D, initially $ABCD = X_3X_2X_1X_0$

If $Y = 0$, at each time: $D_A = B$, $D_B = C$, $D_C = D$, $D_D = A$

If $Y = 1$, at each time: $D_A = D$, $D_B = A$, $D_C = B$, $D_D = C$

Basically, Y is used as switch between 2 options for each D flip-flops. This can be solved using a 2-to-1 multiplexer for each flip-flop.

$D_A = (\overline{Y} \cdot B) + (Y \cdot D)$

$D_B = (\overline{Y} \cdot C) + (Y \cdot A)$

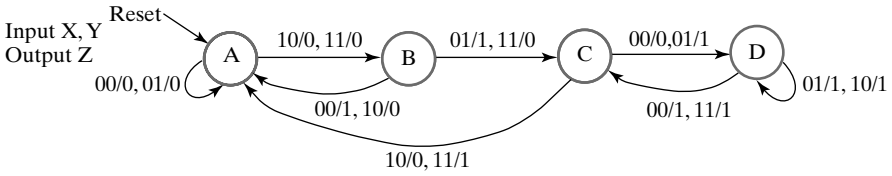
$D_C = (\overline{Y} \cdot D) + (Y \cdot B)$

$D_D = (\overline{Y} \cdot A) + (Y \cdot C)$

Circuit:

… I think at this point it should be simple enough.

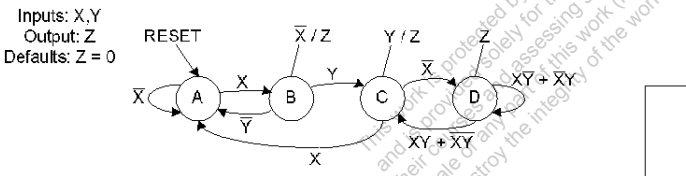
3. Find a state-machine diagram that is equivalent to the following state diagram. Reduce the complexity of the transition conditions as much as possible. Attempt to make outputs unconditional by changing Mealy outputs to Moore outputs. Make a state assignment to your state-machine diagram and find an implementation for the corresponding sequential circuit using D flop-flops, AND gates, OR gates, and inverters.

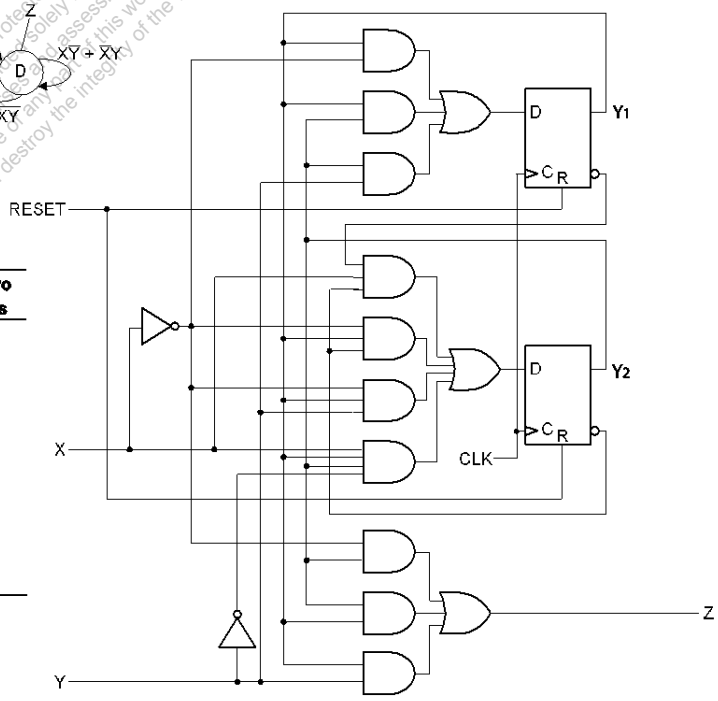


(1) Draw the state-machine diagram.

(2) Write down the Flip-Flop Input Equations and Output Equations.

(3) Implement the circuit, save as `circuit3.cct` .





State table:

State	State Code	Transition Condition	Next State	State Code	Non-zero Outputs
A	00	$\bar{X}$	A	00	
		X	B	01	
B	01				$\bar{X}$ / Z
		$\bar{Y}$	A	00	
		Y	C	10	
C	10				Y / Z
		$\bar{X}$	D	11	
		X	A	00	
D	11				Z
		$X\bar{Y} + \bar{X}Y$	D	11	
		$XY + \bar{X}\bar{Y}$	C	10	