



CSCI 150

Introduction to Digital and Computer System Design

Lecture 4: Sequential Circuit VI

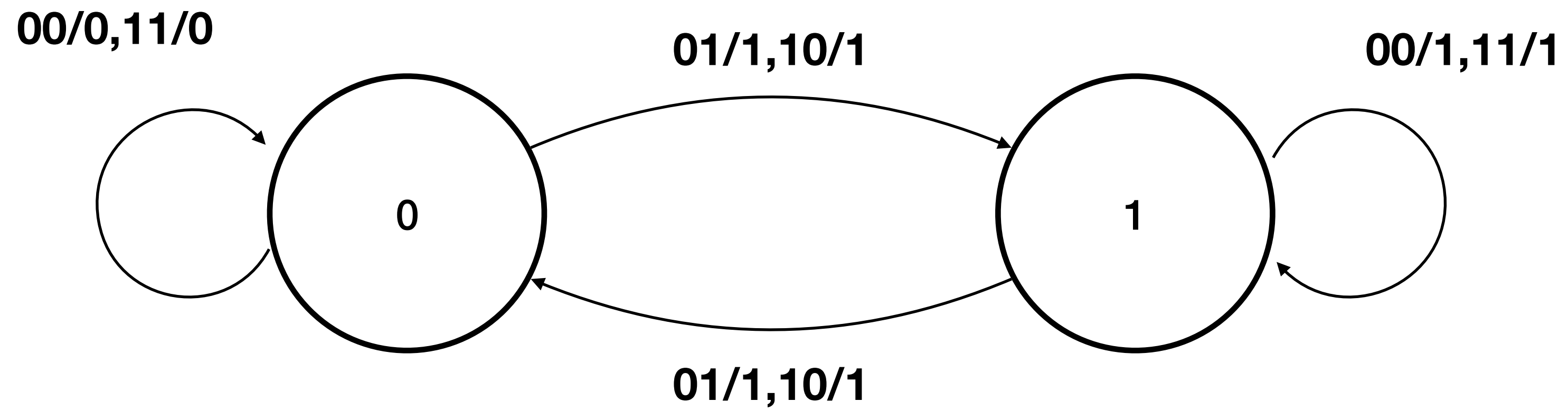


Jetic Gū
2020 Winter Semester (S1)

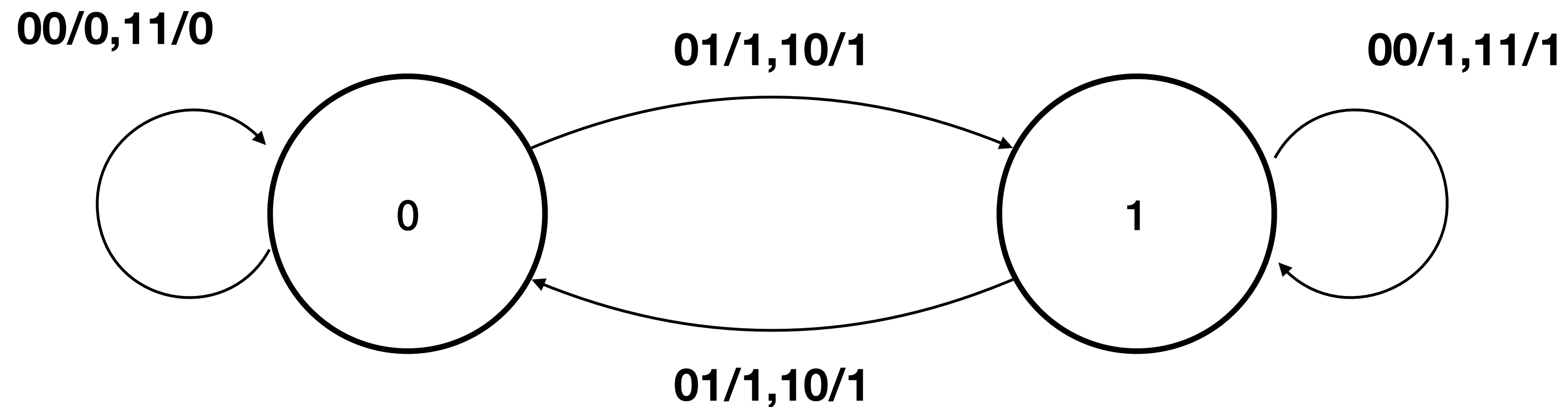
Overview

- Focus: Basic Information Retaining Blocks
- Architecture: Sequential Circuit
- Textbook v4: Ch5 5.7; v5: Ch4 4.6
- Core Ideas:
 1. State Machine Diagrams: Moore model

State Diagram

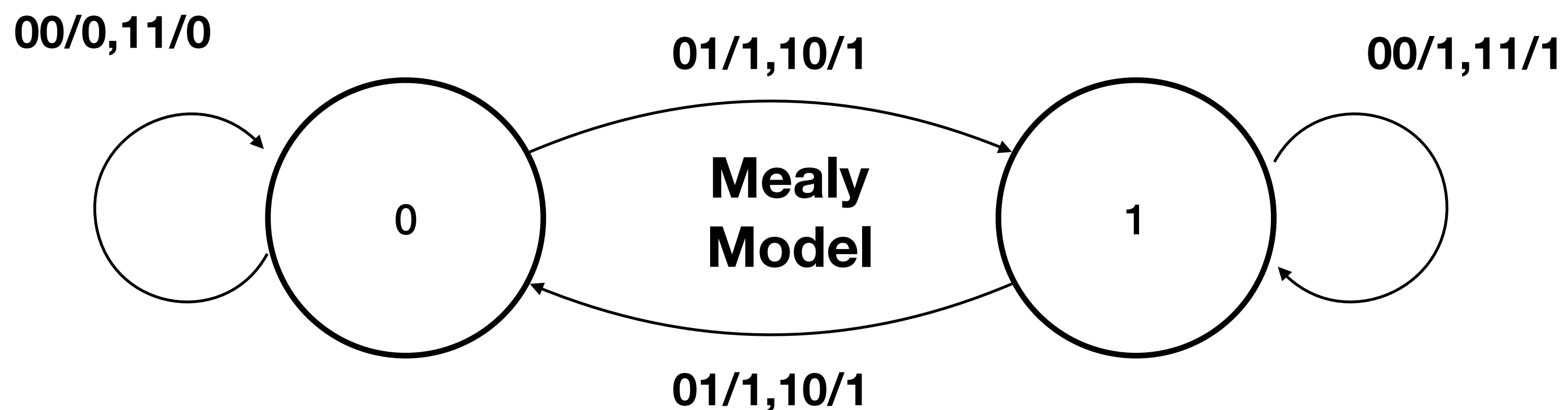


State Diagram



Mealy machine: a finite-state machine whose output values are determined both by its current state and the current inputs

State Diagram



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State Diagram

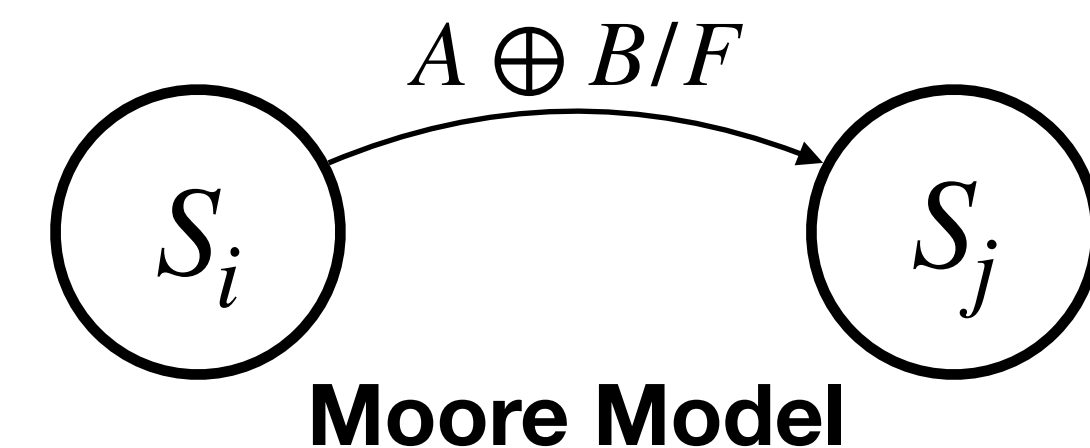
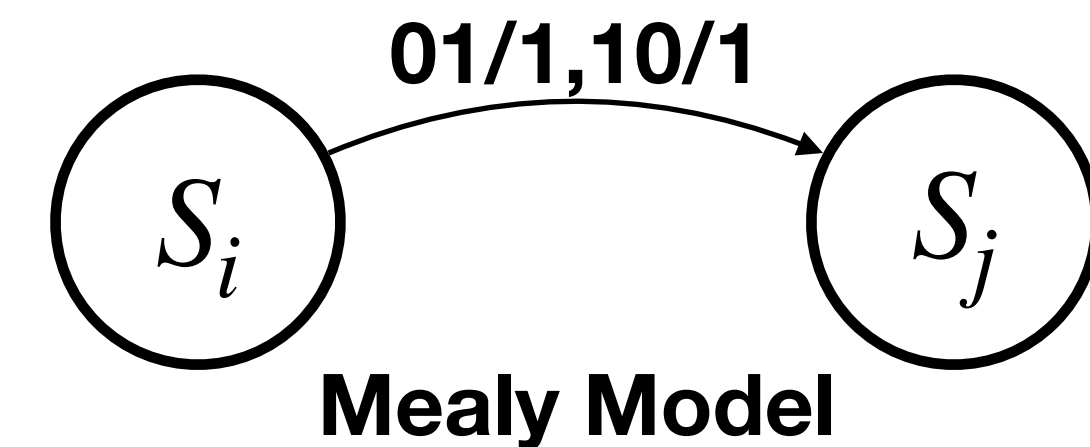
- Modelling state transitions in a visual way
- Problems with Mealy Model
 - Inefficient when input and output contain too many bits
all 2^n inputs and m -bit outputs must be written down for each transition
 - Unworkable for larger designs

State Machine Diagrams

Moore Model

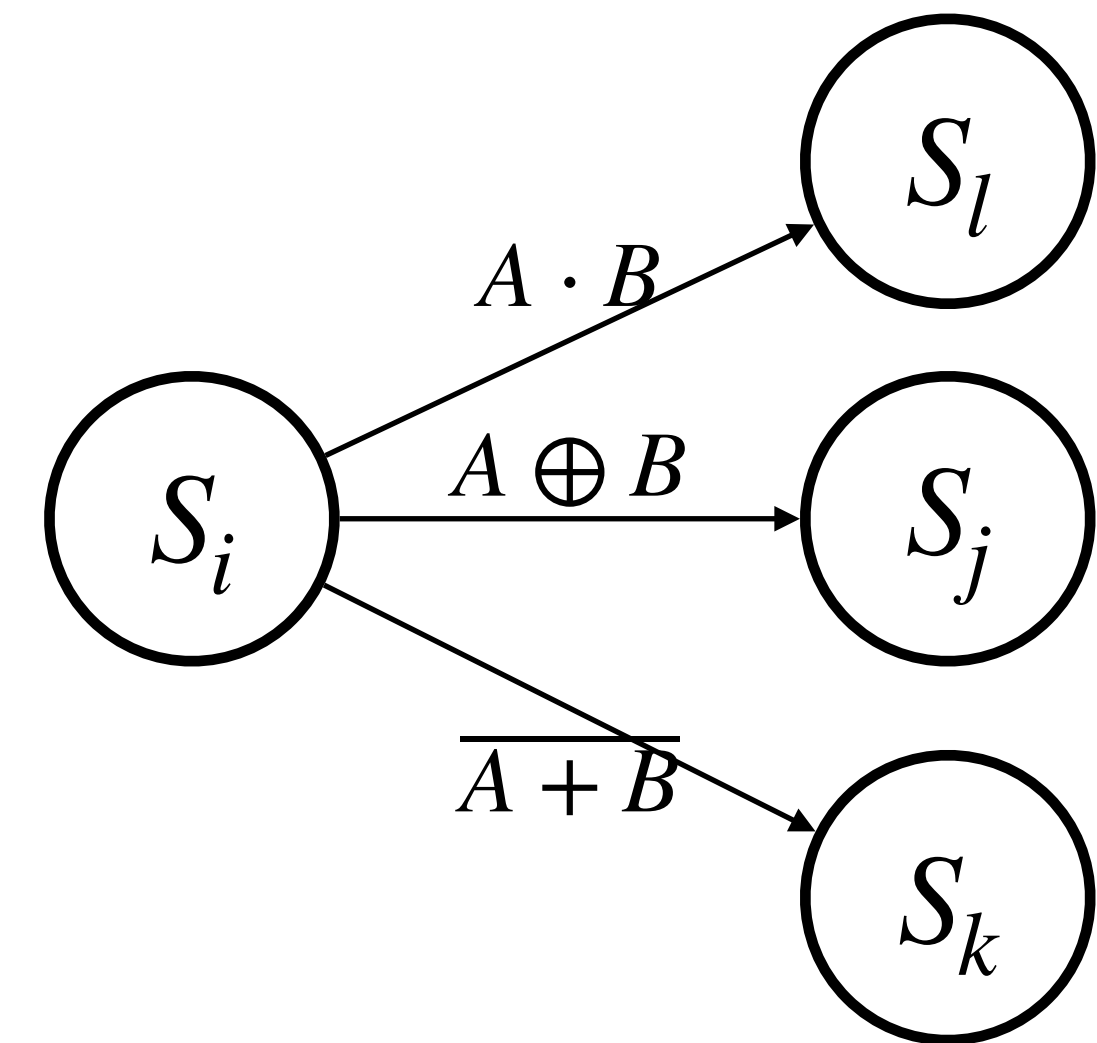
Improvements over Mealy

- Called Moore, the name sounds better (also State-Machine Diagram)
- Conditions
 - Input Condition: Boolean expressions or equations
Also called **transition condition (TC)**, causes transition when its value is 1
 - **Output Condition (OC)**: Boolean expressions or equations
Causes specific output when its value is 1



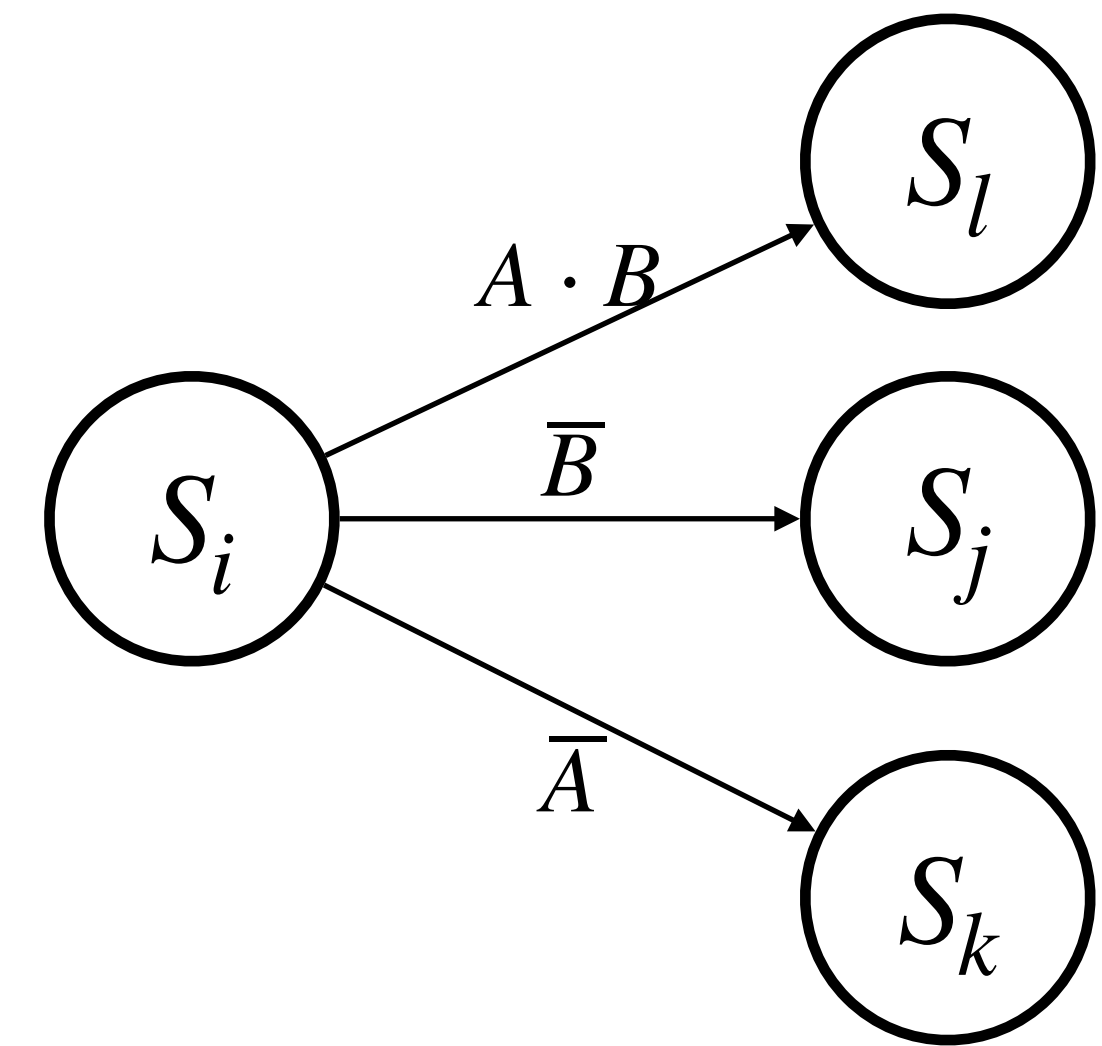
Transition Conditions

- Associated with transitions
- Performs transition when condition is met
- Validity
Must not be conflicting conditions
i.e. only one TC can be true for any given input



Transition Conditions

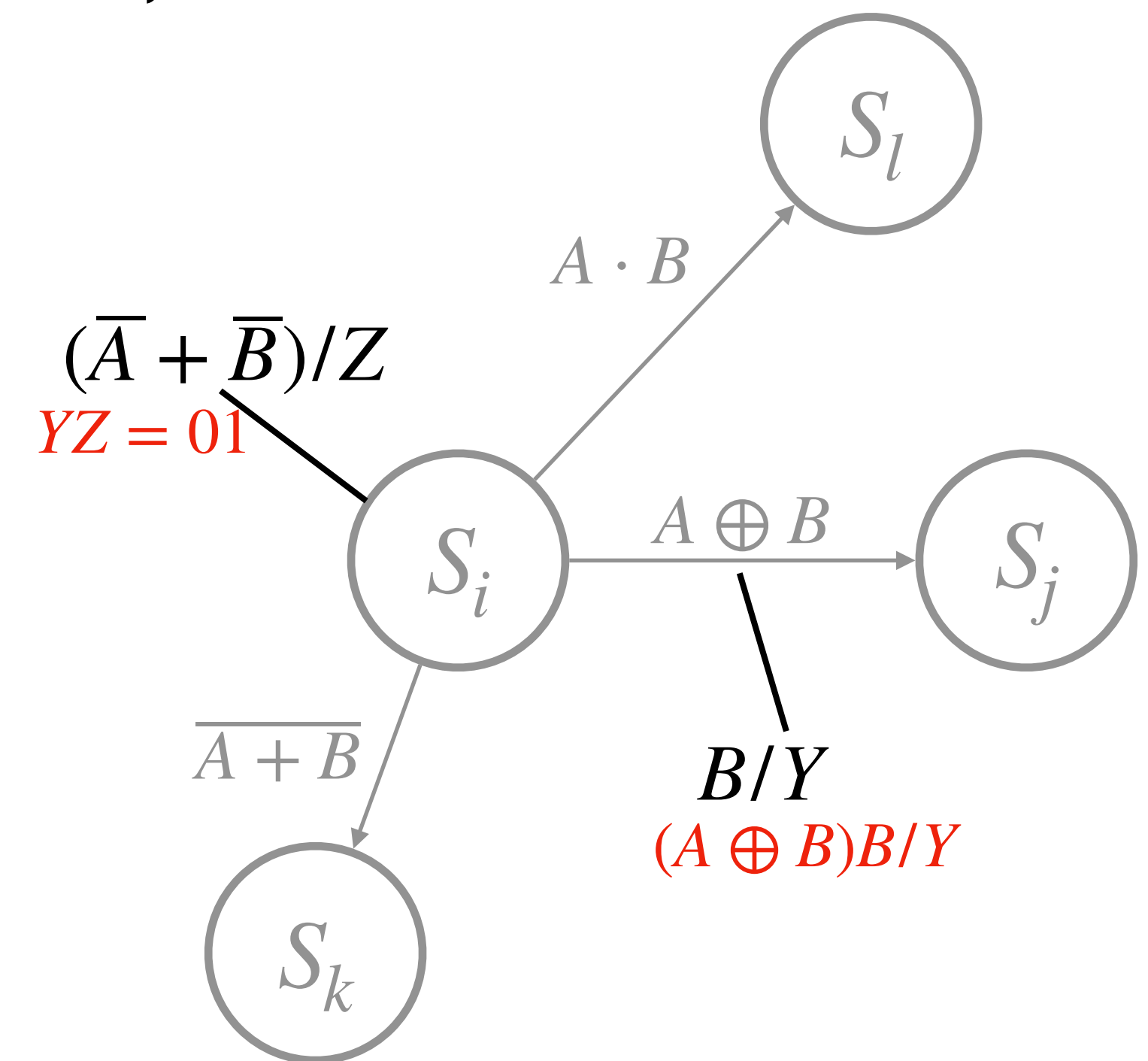
- Invalid TC
 - Condition \bar{A} and \bar{B} can be met at the same time
- Check all transitions from each state of invalid TC



Output Conditions

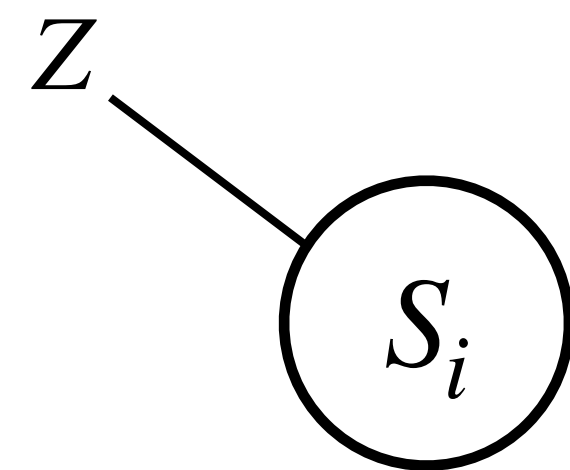
Defaults: $Y = 0, Z = 0$

- Associated with transitions/states
- For associated transition/state, outputs when condition is met
- Default: output values unless otherwise specified
- Validity
Must not be conflicting conditions
i.e. only one OC can be true for any given input/state

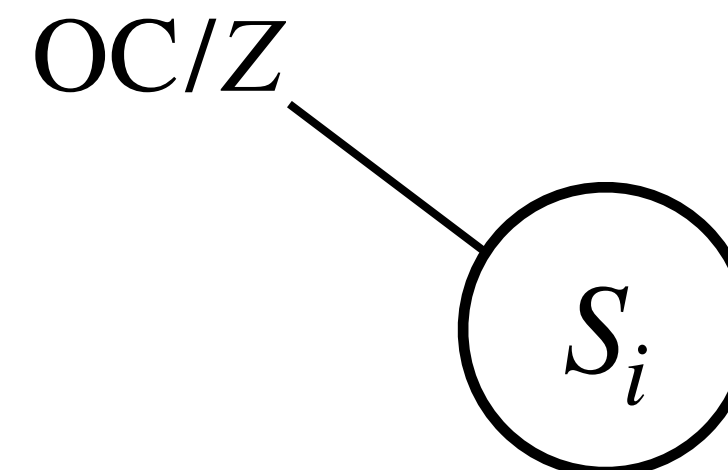


Output Conditions

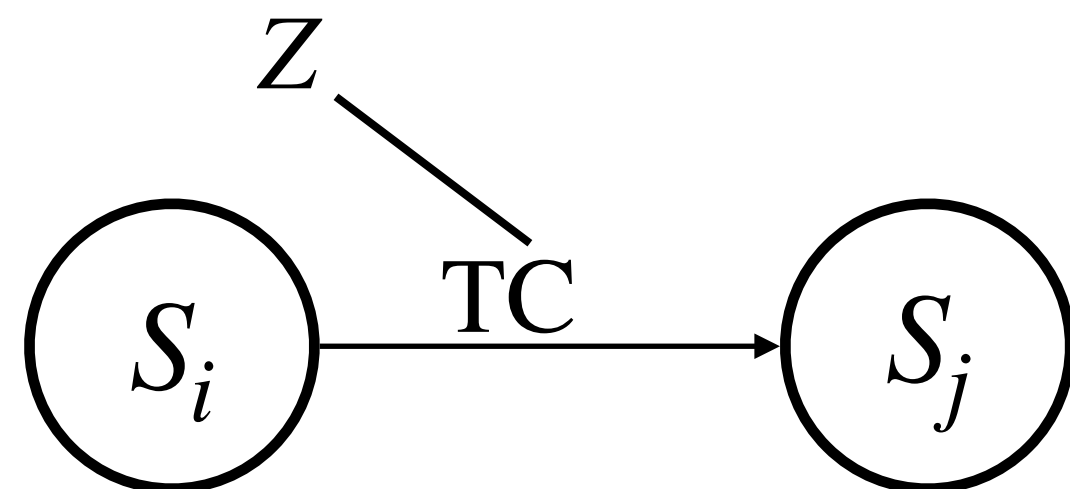
Defaults: $Y = 0, Z = 0$



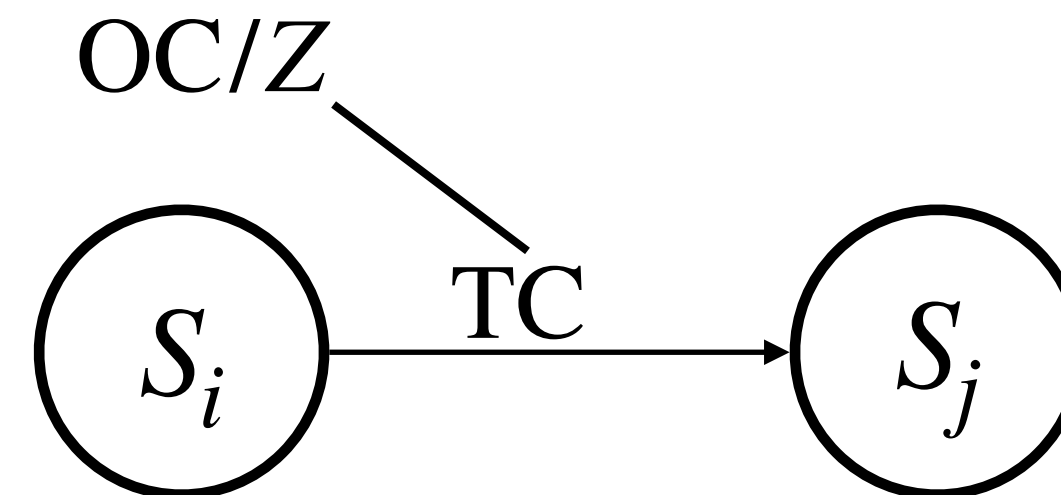
Always output 01 at state S_i



Output 01 when condition OC is met at S_i



Always output 01 at state S_i ,
when input meets TC

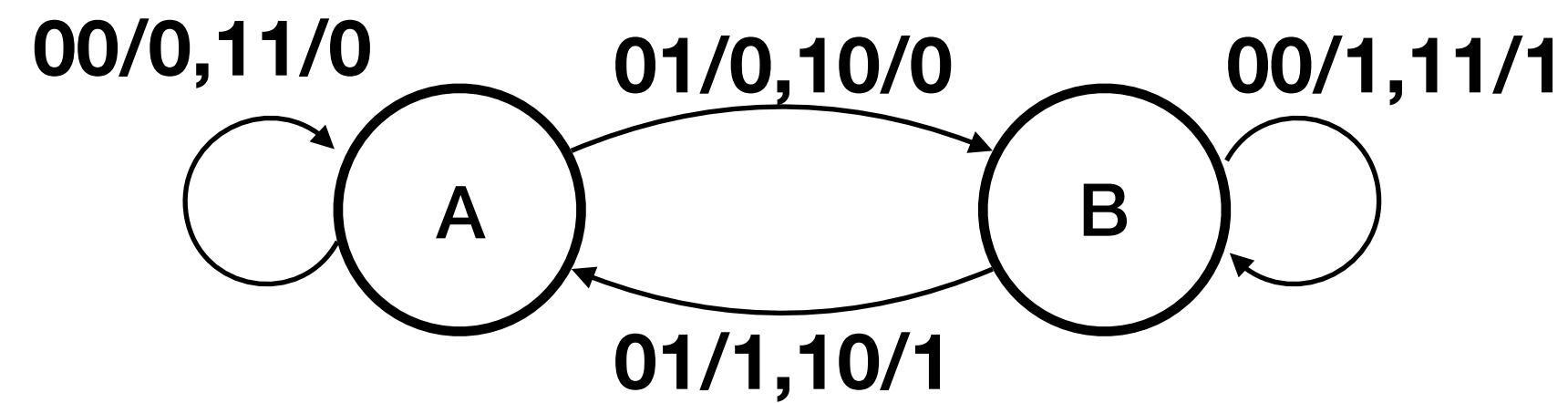


Output 01 when condition OC is met at S_i ,
and input meets TC

Output Conditions

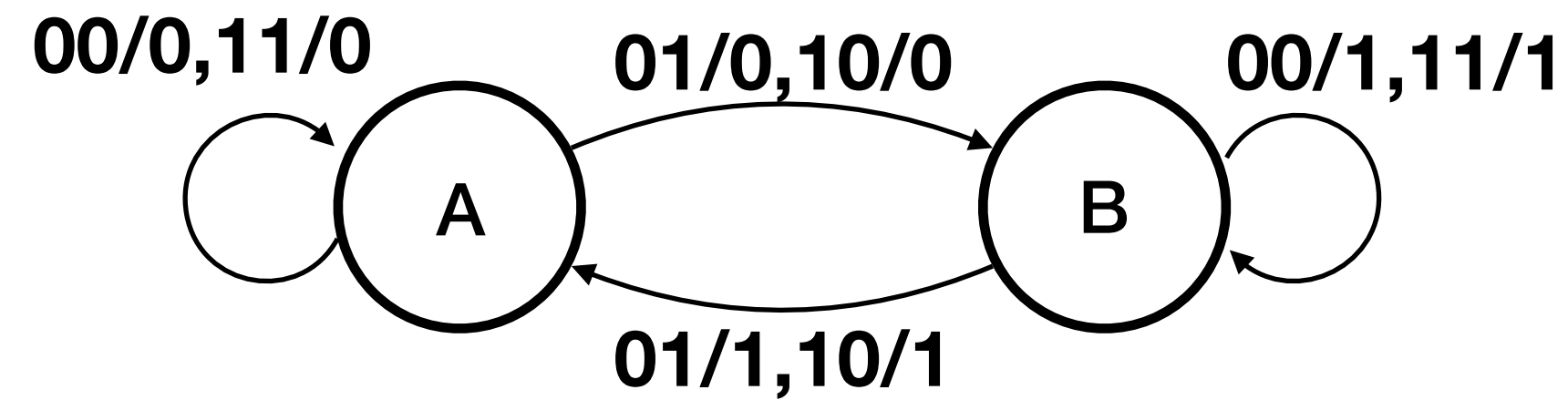
- Invalid OC
 - Condition \bar{A} and \bar{B} can be met at the same time
- Check all transitions from each state of invalid OC

From Mealy to Moore

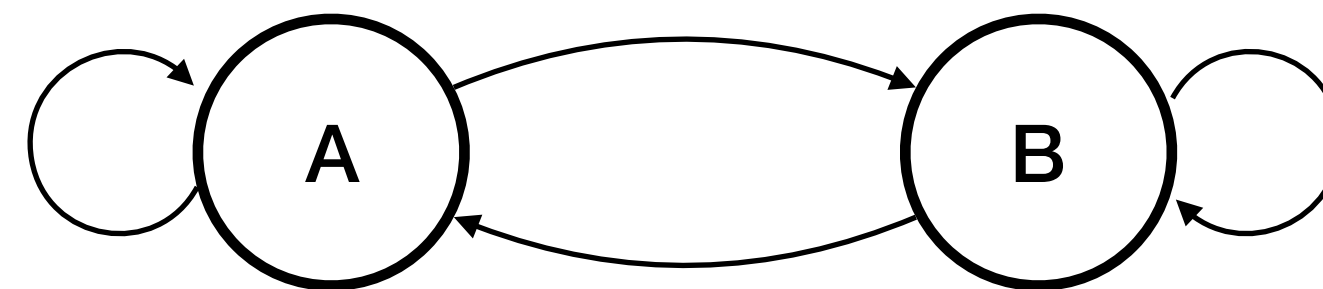


1. Preserve arcs
2. Do the TCs
3. Do the OCs

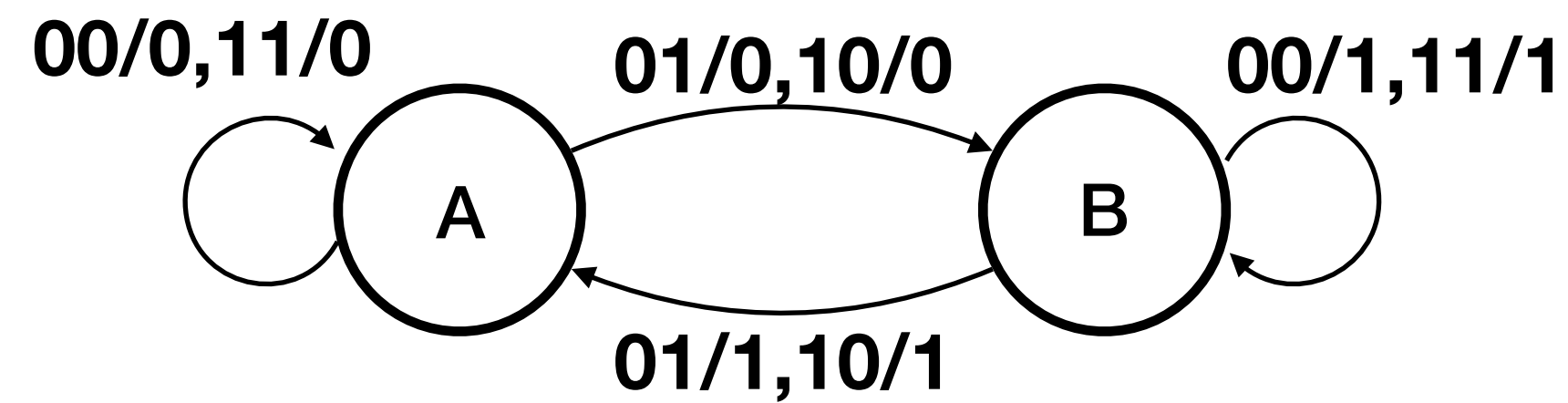
From Mealy to Moore



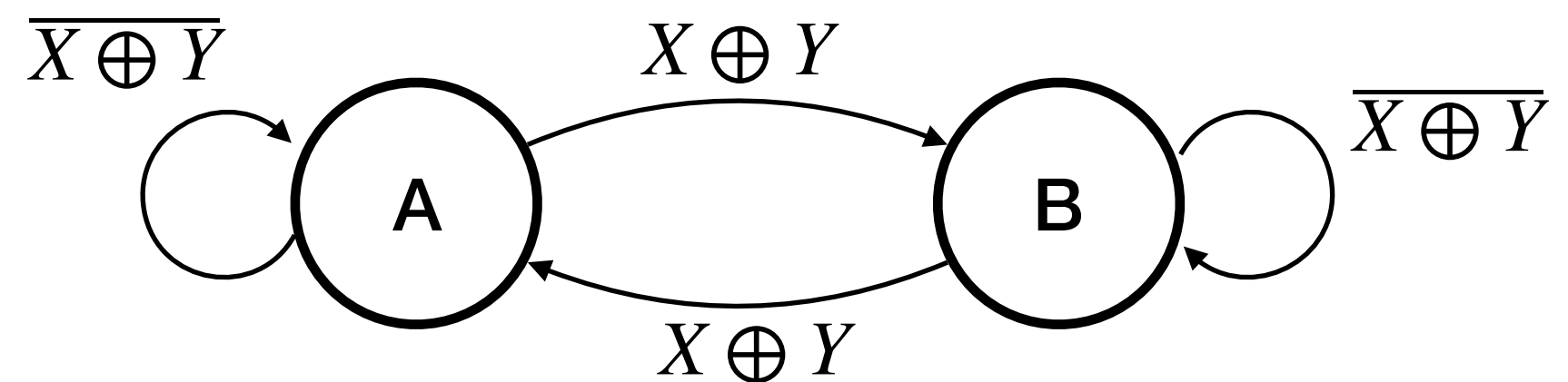
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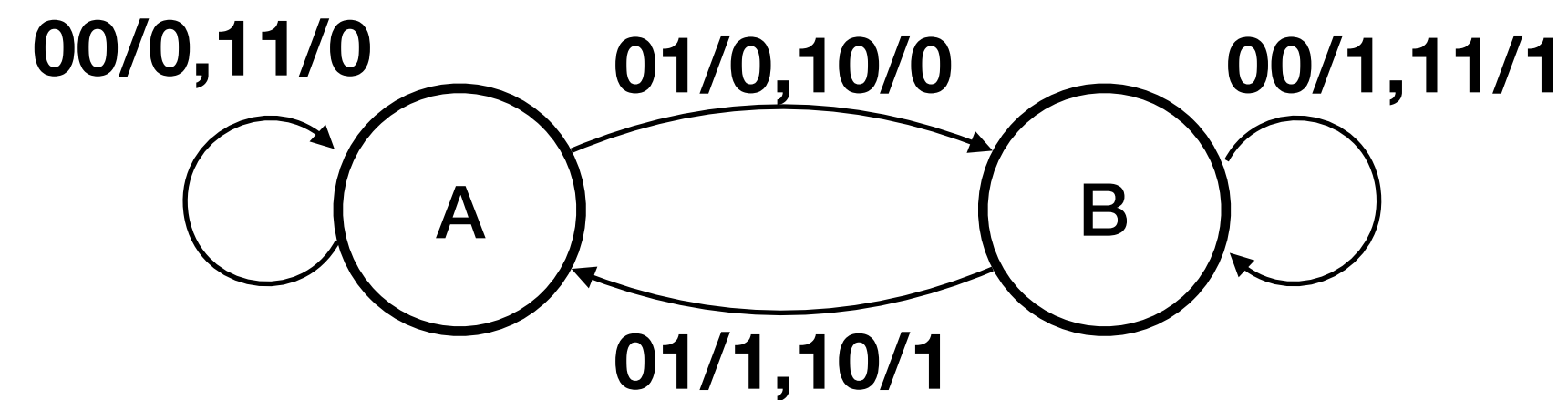
From Mealy to Moore



1. Preserve arcs
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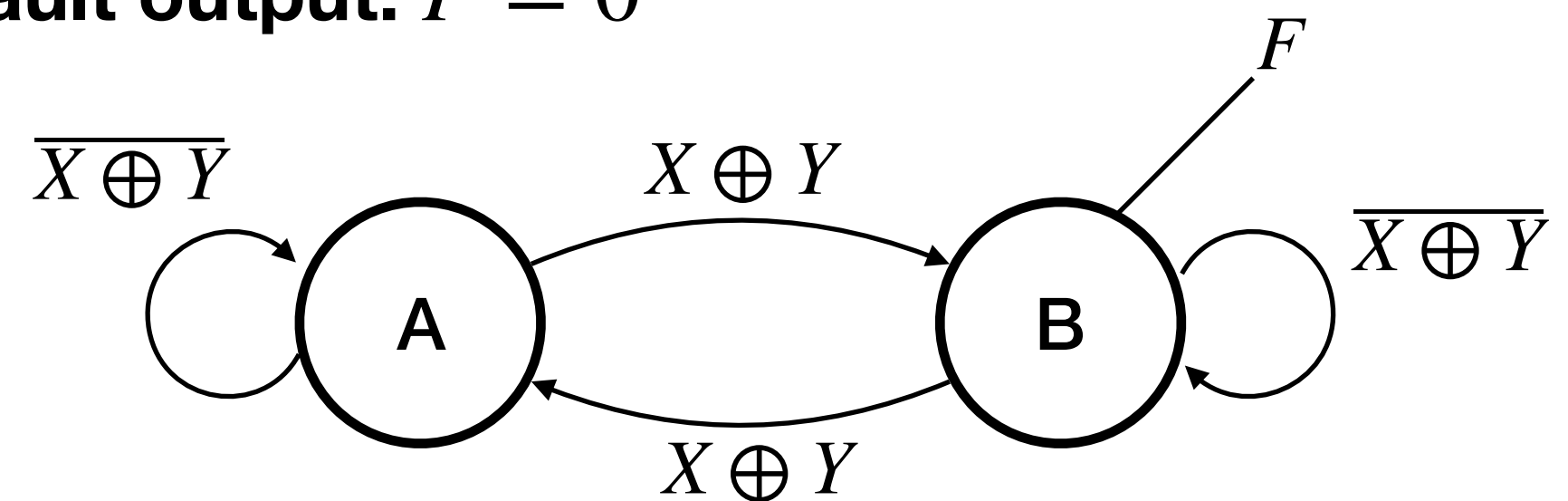


From Mealy to Moore



1. Preserve arcs
2. Do the TCs
3. Do the OCs

Default output: $F = 0$



From State Table to Moore

State Table

Present State		X	Next State		F
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

From State Table to Moore

State Table

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0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

Input: X

Output: F

Default: $F = 0$

Exercise

From State Table to Moore

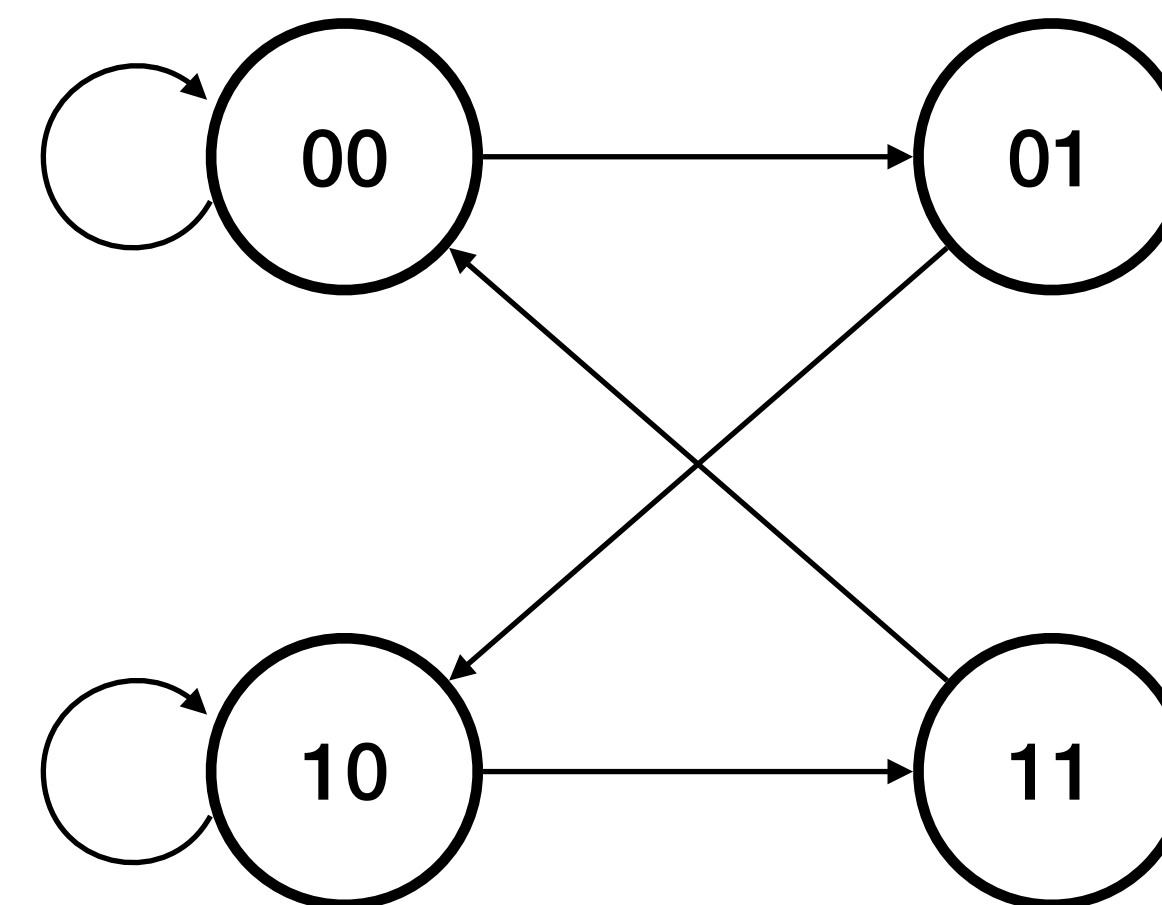
State Table

Present State		X	Next State		F
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

Input: X

Output: F

Default: $F = 0$



From State Table to Moore

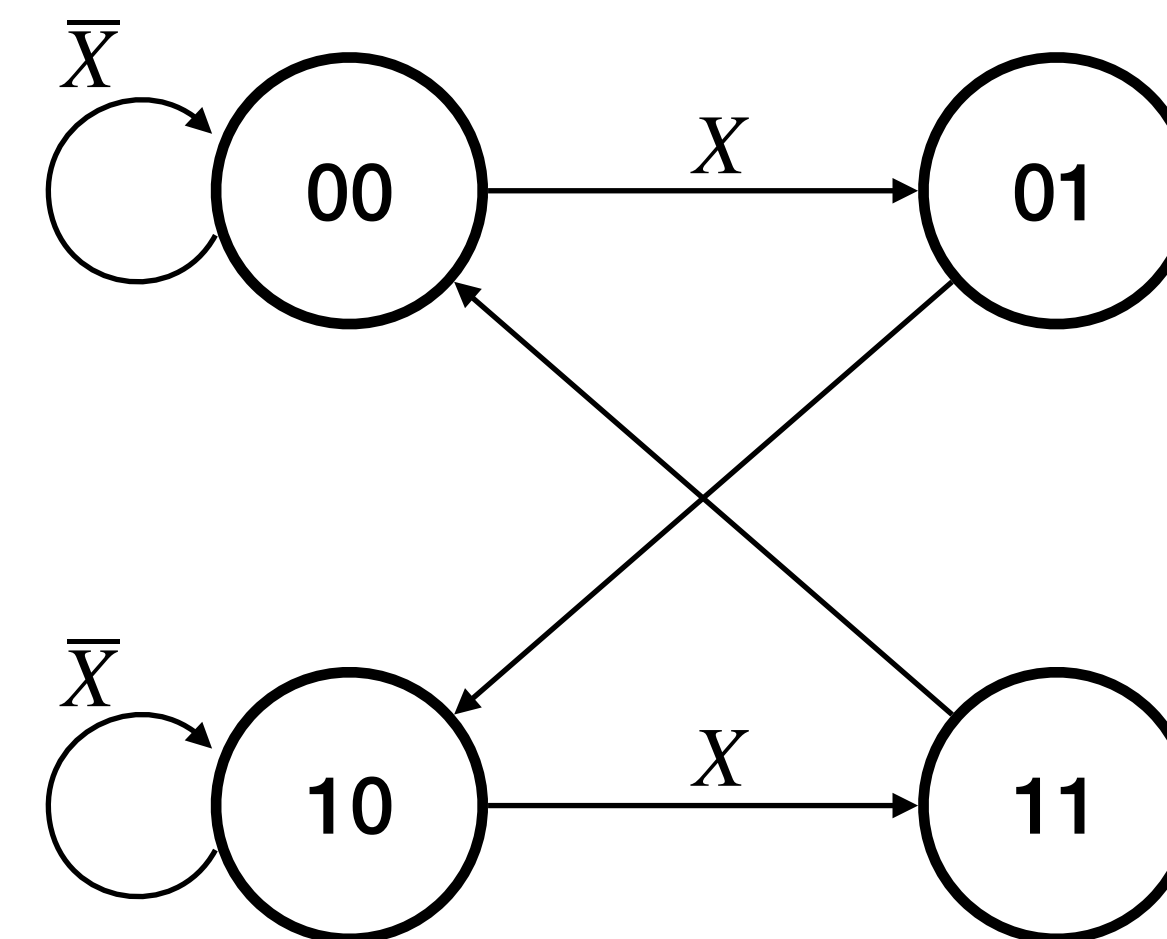
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1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

Input: X

Output: F

Default: $F = 0$



From State Table to Moore

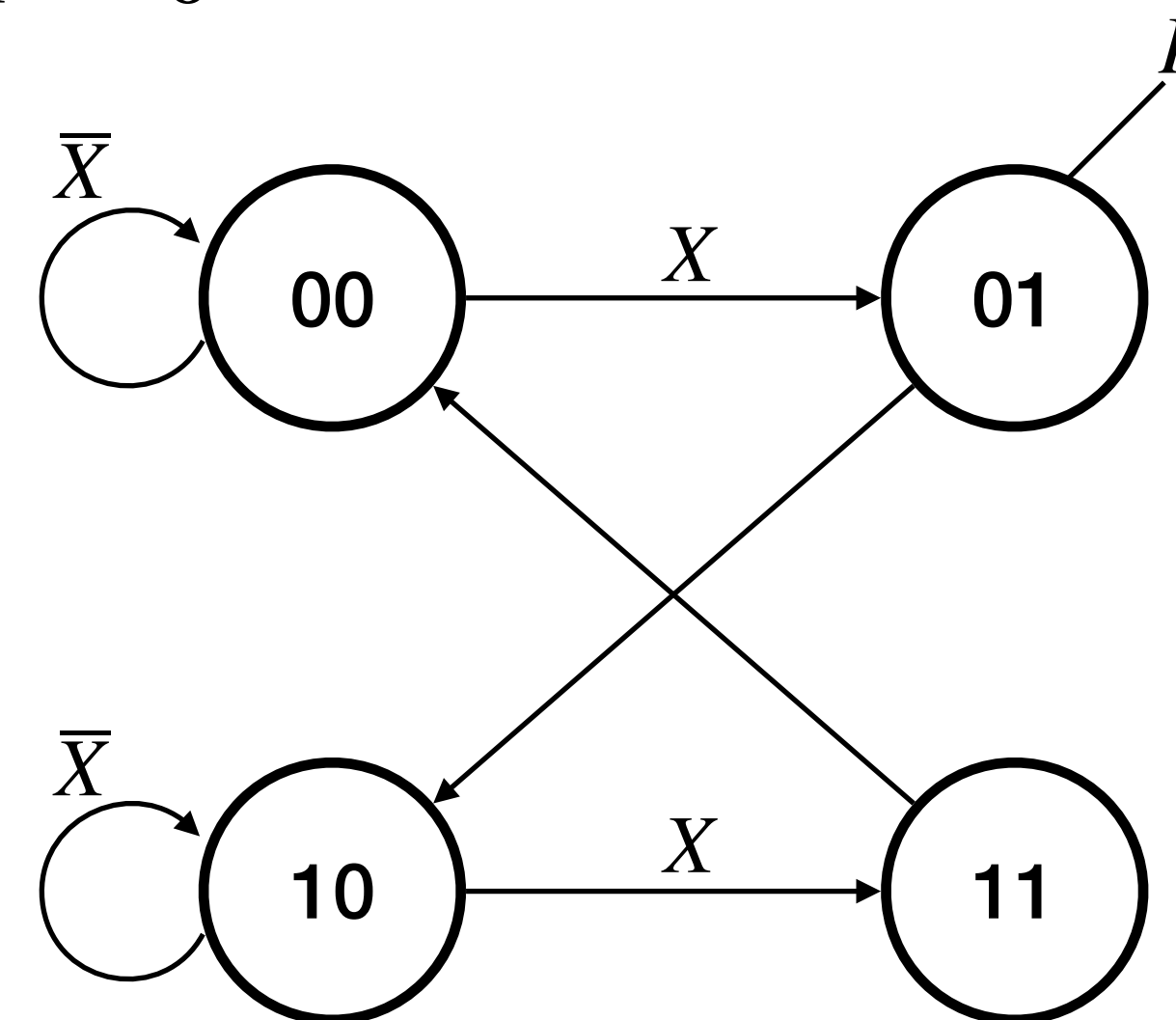
State Table

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0	0	1	0	1	0
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0	1	1	1	0	1
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1	1	0	0	0	0
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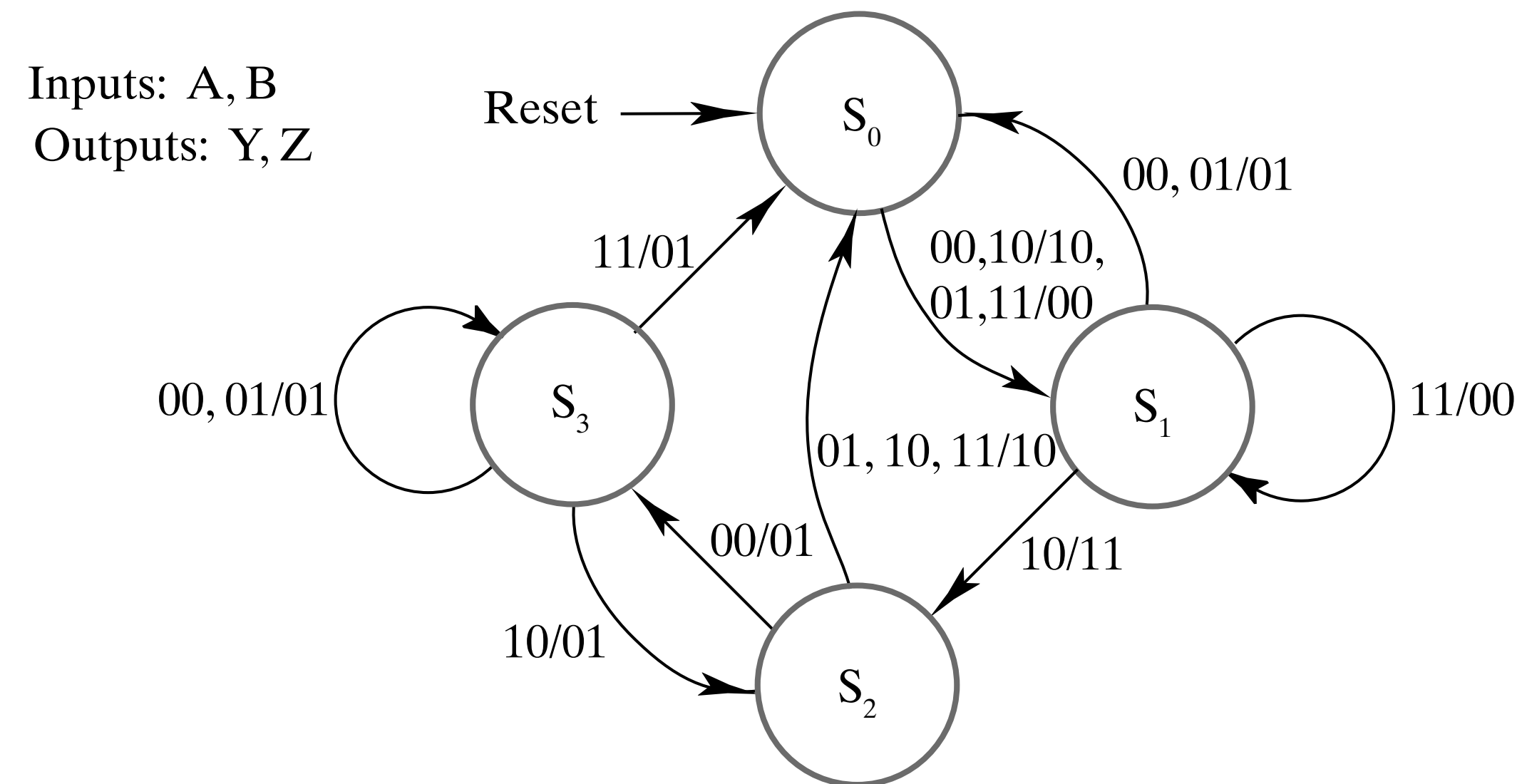
Input: X

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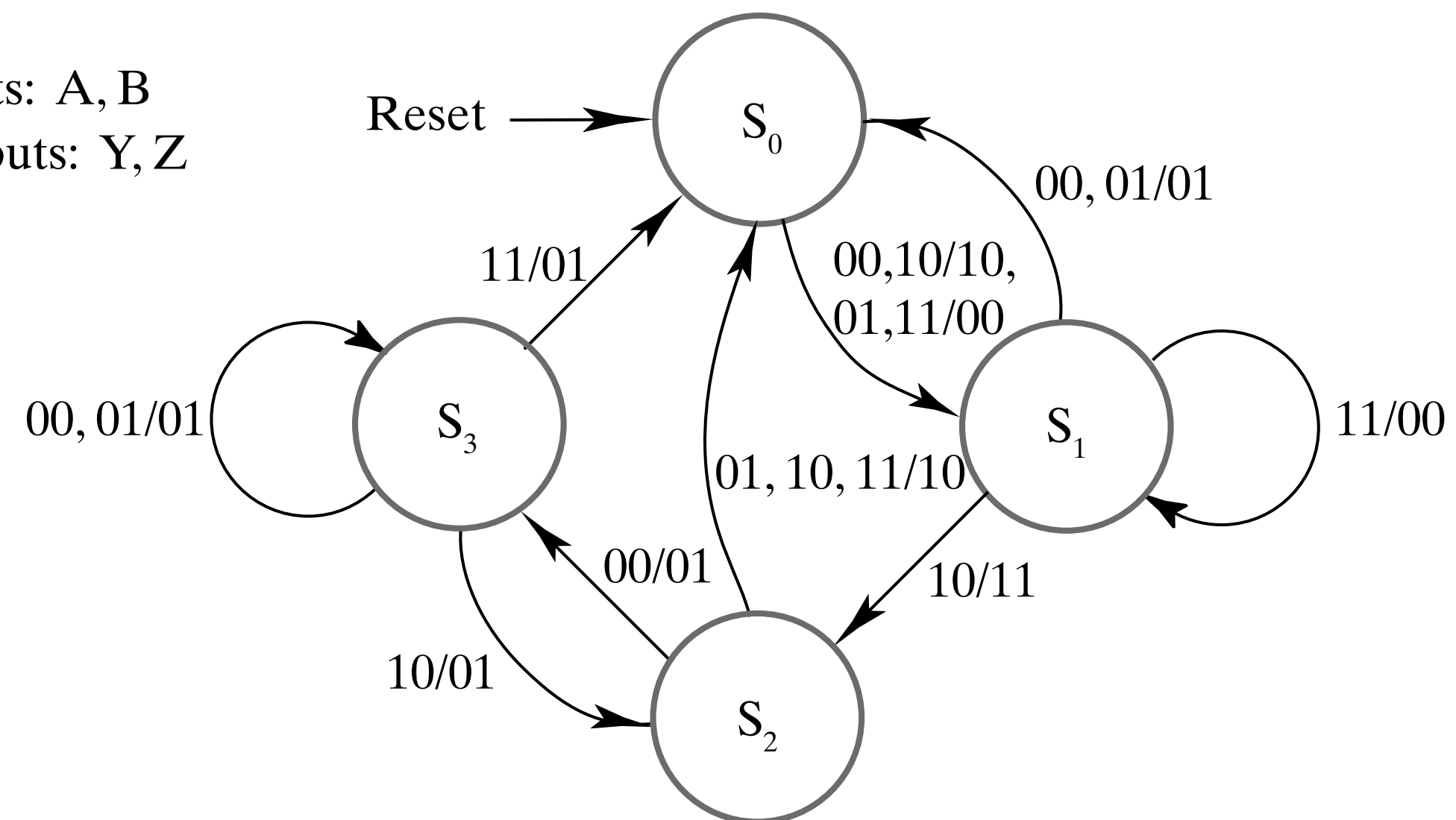


From Mealy to Moore

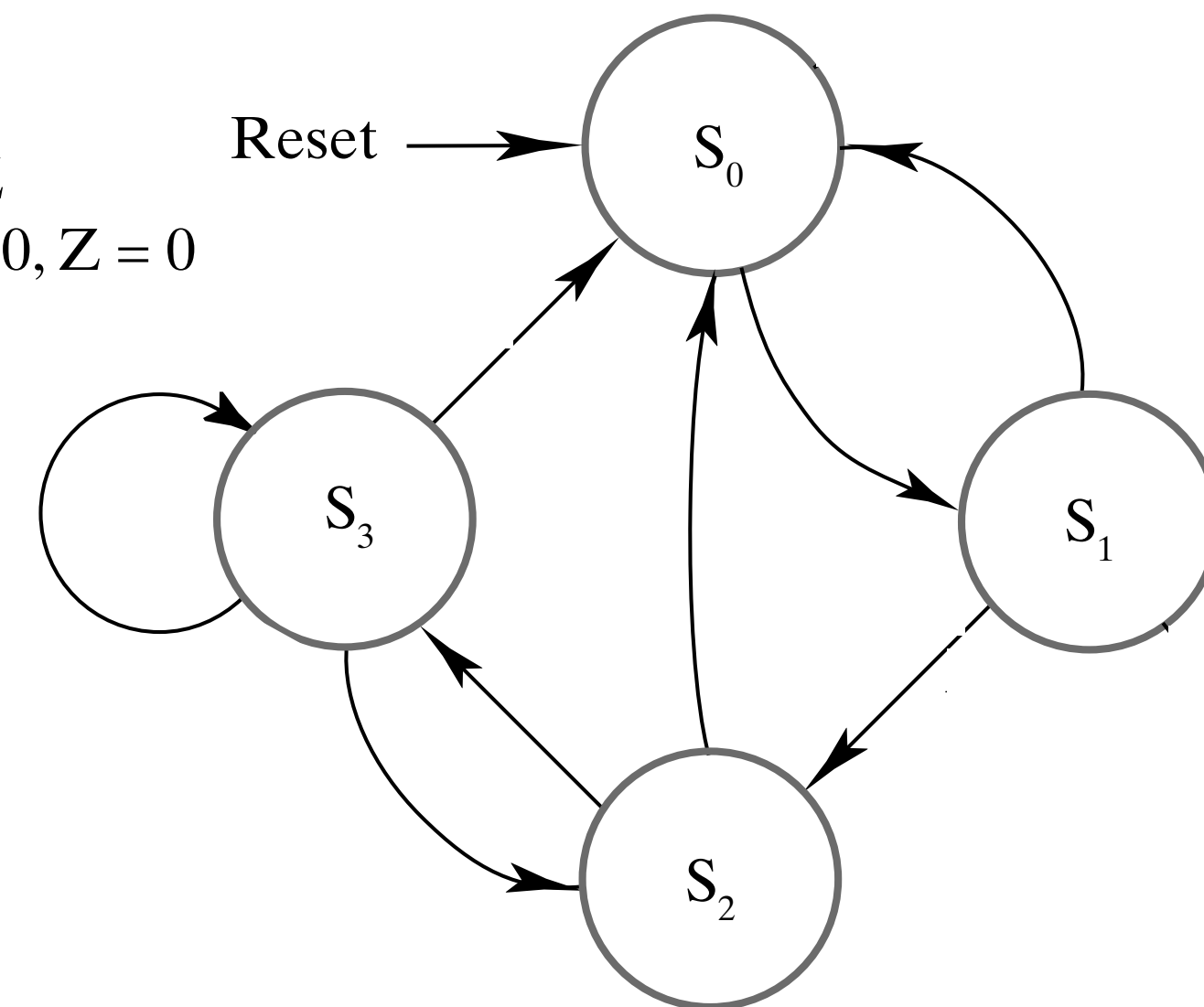


From Mealy to Moore

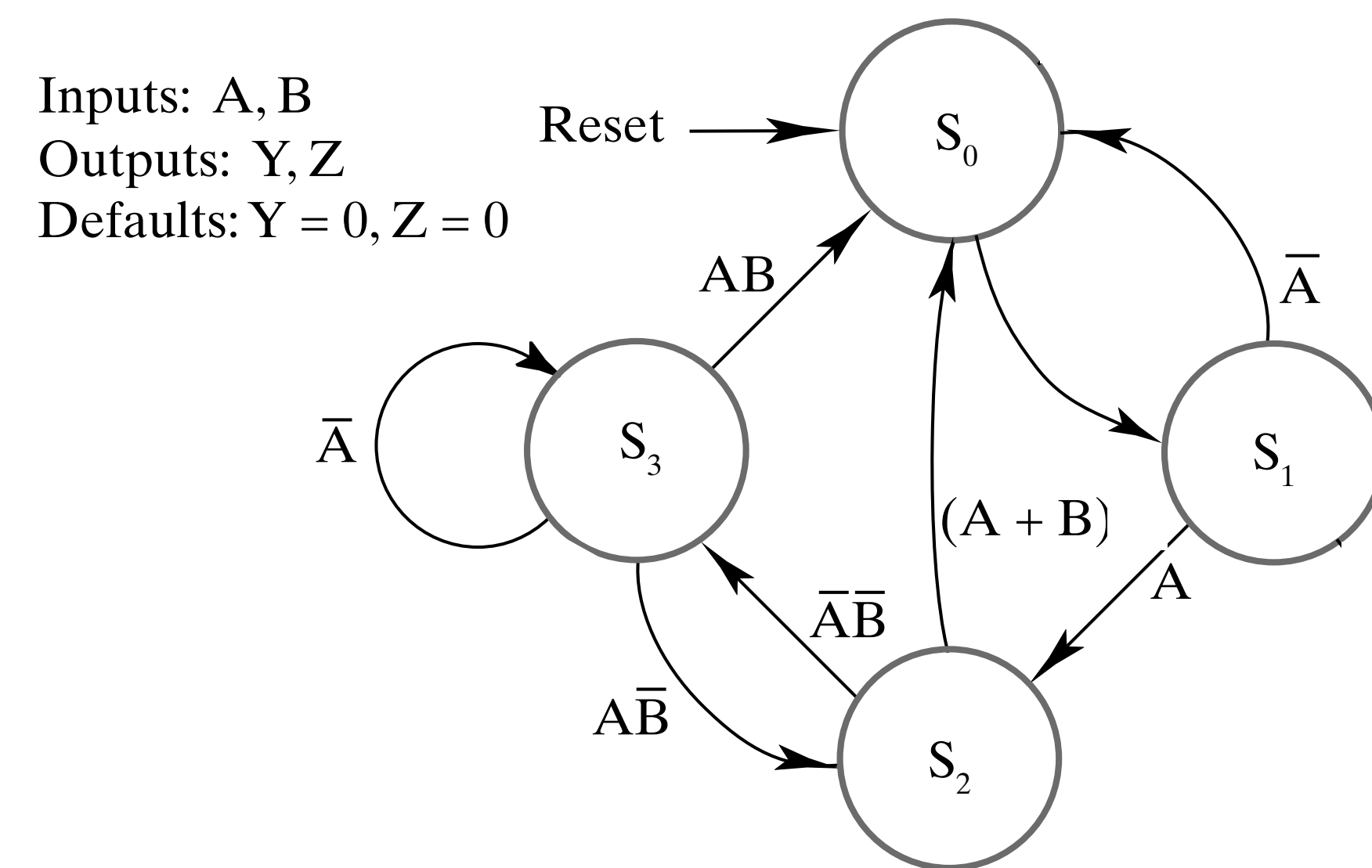
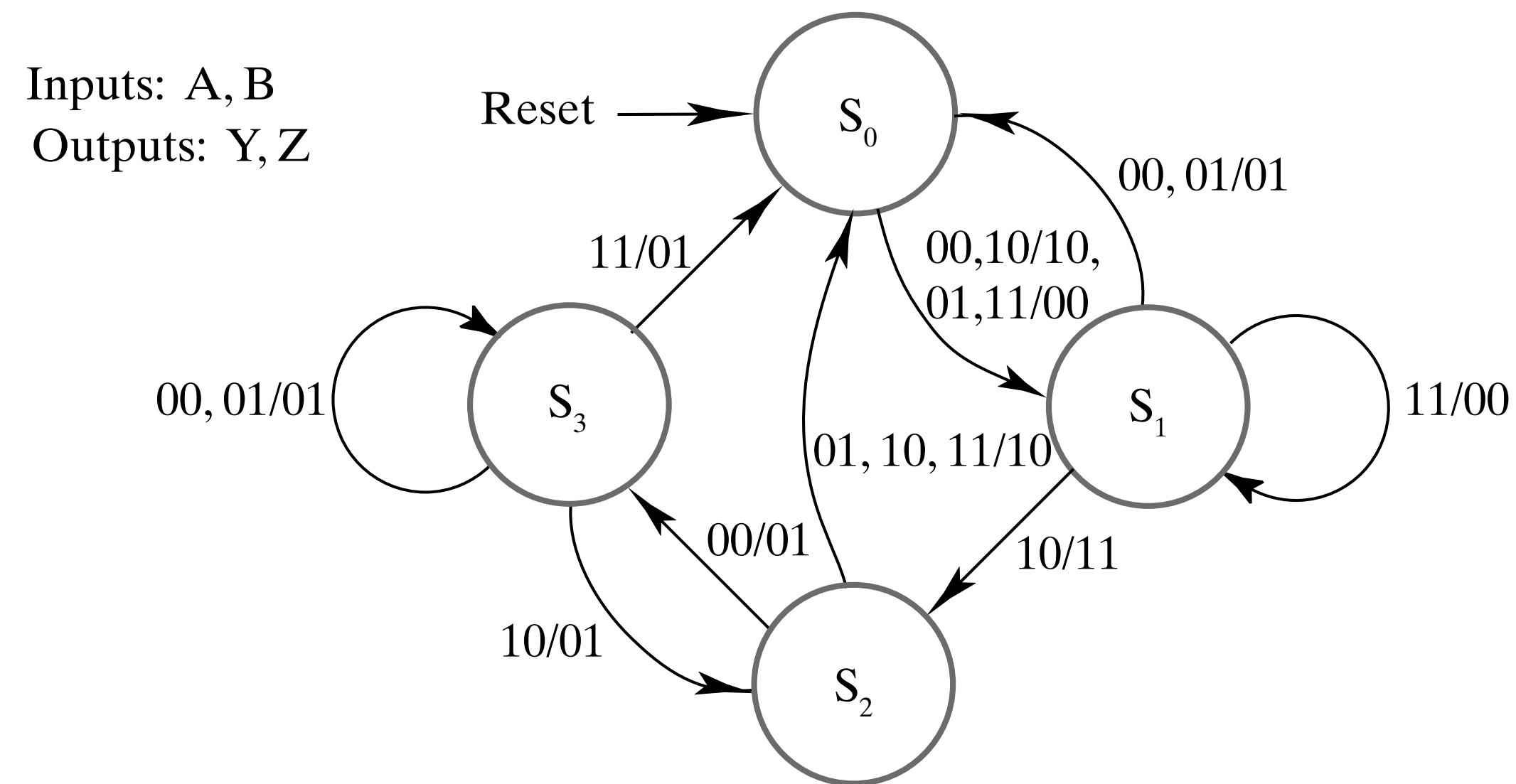
Inputs: A, B
Outputs: Y, Z



Inputs: A, B
Outputs: Y, Z
Defaults: Y = 0, Z = 0

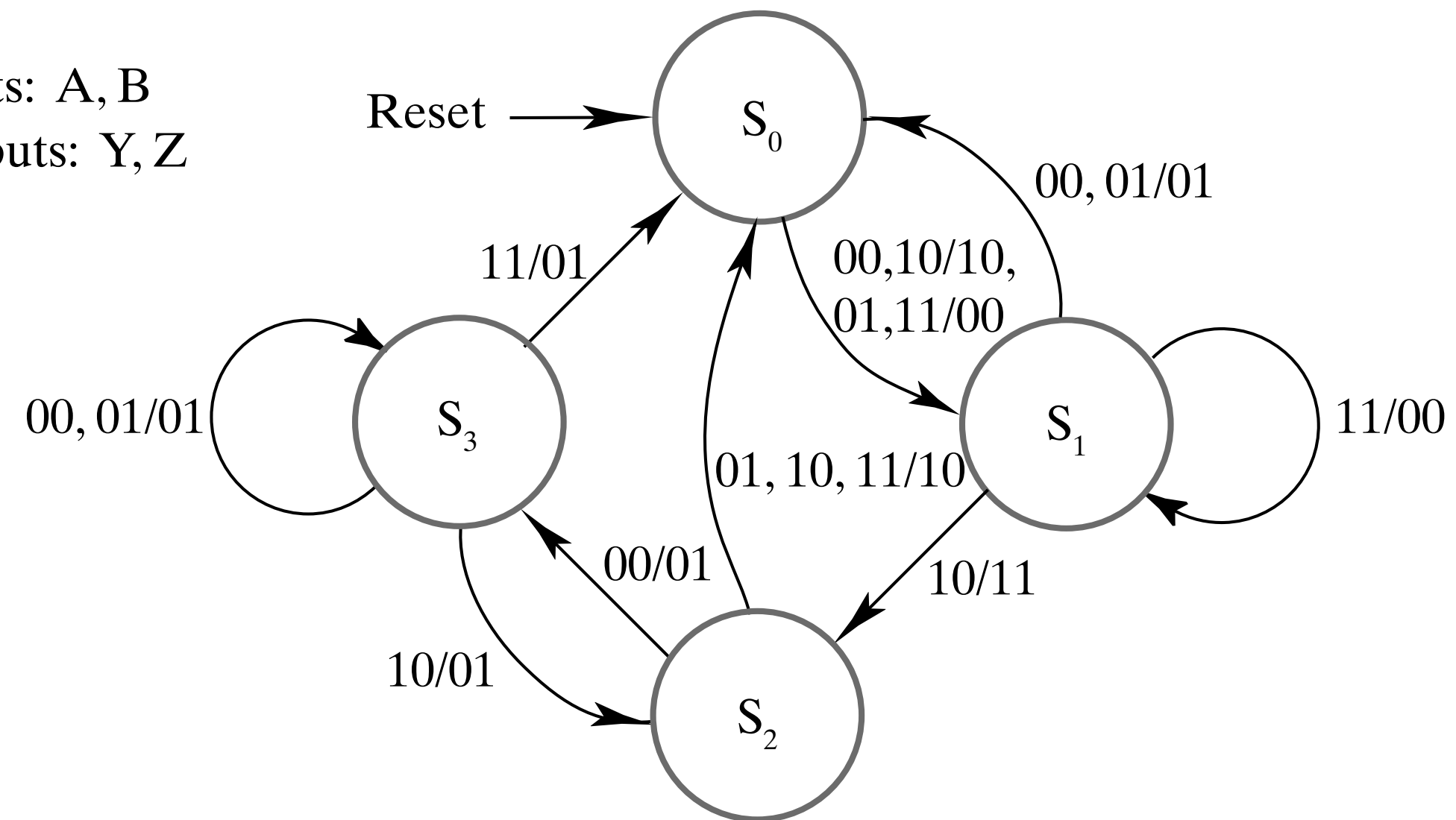


From Mealy to Moore



From Mealy to Moore

Inputs: A, B
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Outputs: Y, Z
Defaults: $Y = 0, Z = 0$

