Jetic Gū
Columbia College

This assignment is due on 23 Feb. 2020

Please remember to write your name and student number.

Please submit a single PDF for each assignment. Handwritten submissions and proprietary formats (e.g. Pages or MS Word) will not be accepted. The Lab portion must be submitted separately.

Assignment 3 Answers

1. Design a combinational circuit that accept a 3-bit number and generates a 6-bit binary number output equal to the square of the input number.

   A. Write down the specification (input, output variables, and their relation).

   Input: 3-bit binary number X_2, X_1, X_0

   Output: 6-bit binary number $Y_5, Y_4, Y_3, Y_2, Y_1, Y_0$

   B. Formulation write down the relations in boolean algebra or truth table.

X_2	X_1	X_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

$$Y_5 = \Sigma m(6,7)$$

$$Y_4 = \Sigma m(4,5,7)$$

$$Y_3 = \Sigma m(3,5)$$

$$Y_2 = \Sigma m(2,6)$$

$$Y_1 = 0$$

$$Y_0 = \Sigma m(1,3,5,7)$$

   C. Perform optimisation to simplify the design.

$$Y_5 = X_2 X_1$$

$$Y_4 = X_2\overline{X_1\overline{X_0}}$$
$$Y_3 = (X_2\overline{X_1} + \overline{X_2}X_1)X_0$$
$$Y_2 = (X_2\overline{X_1} + \overline{X_2}X_1)\overline{X_0}$$
$$Y_1 = 0$$
$$Y_0 = X_0$$

D. Perform technology mapping using AND, OR, NOT gates, draw the logical diagram.

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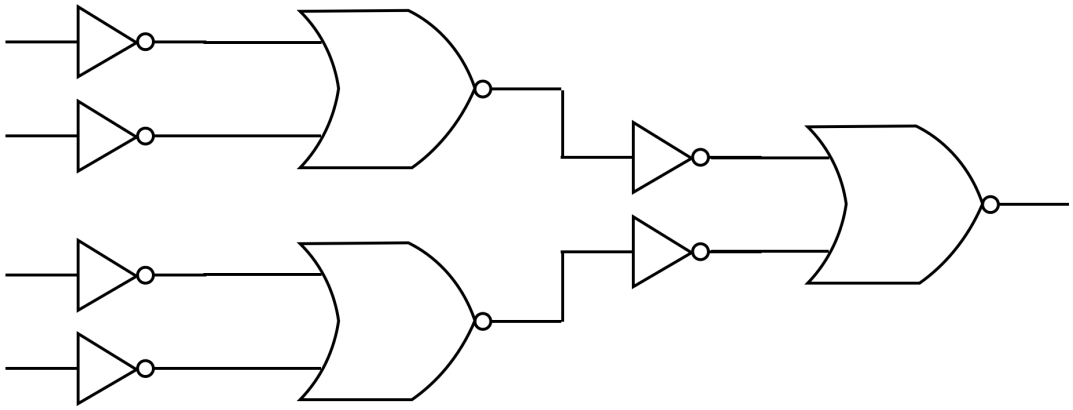
2. Design a 4-input AND gate using 2-input NOR gates and NOT gates, and draw the circuit diagram.



3. A traffic metering system for controlling the release of traffic from an entrance ramp onto a superhighway has the following specifications for a part of its controller. There are three parallel metering lanes, each with its own stop (red)–go (green) light. One of these lanes, the car pool lane, is given priority for a green light over the other two lanes. Otherwise, a “round robin” scheme in which the green lights alternate is used for the other two (left and right) lanes. The part of the controller that determines which light is to be green (rather than red) is to be designed. The specifications for the controller follow:

Inputs

PS	Car pool lane sensor (car present—1; car absent—0)
LS	Left lane sensor (car present—1; car absent—0)
RS	Right lane sensor (car present—1; car absent—0)
RR	Round robin signal (select left—1; select right—0)

Outputs

PL	Car pool lane light (green—1; red—0)
LL	Left lane light (green—1; red—0)
RL	Right lane light (green—1; red—0)

Operation

1. If there is a car in the car pool lane, PL is 1.
2. If there are no cars in the car pool lane and the right lane, and there is a car in the left lane, LL is 1.

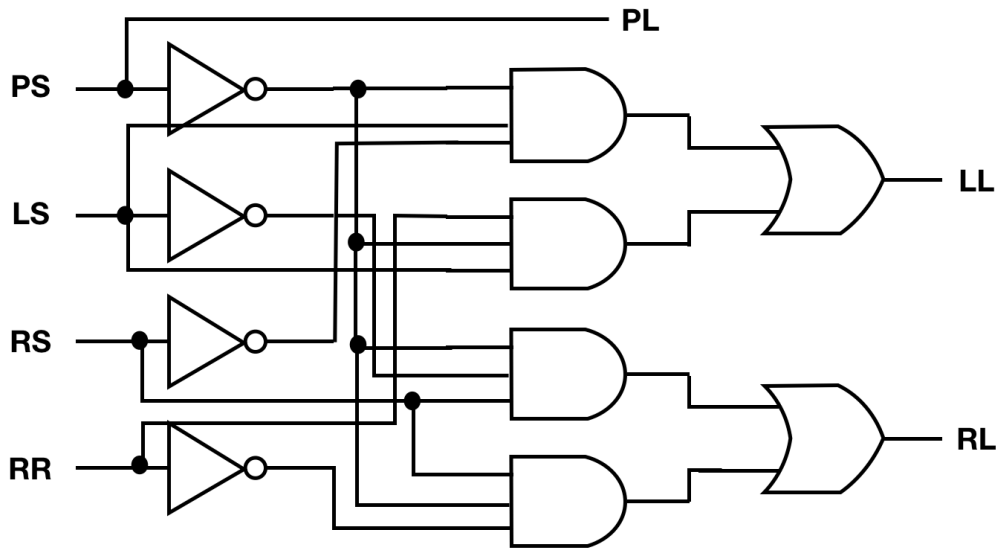
3. If there are no cars in the car pool lane and in the left lane, and there is a car in the right lane, RL is 1.
4. If there is no car in the car pool lane, there are cars in both the left and right lanes, and RR is 1, then LL = 1.
5. If there is no car in the car pool lane, there are cars in both the left and right lanes, and RR is 0, then RL = 1.
6. If any PL, LL, or RL is not specified to be 1 above, then it has value 0.

A. Find the truth table for the controller part.

PS	LS	RS	RR	PL	LL	RL
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	0

$$PL = PS,\ LL = \overline{PS}LS\overline{RS} + \overline{PS}LSRR,\ RL = \overline{PS}\,\overline{LS}RS + \overline{PS}RS\overline{RR}$$

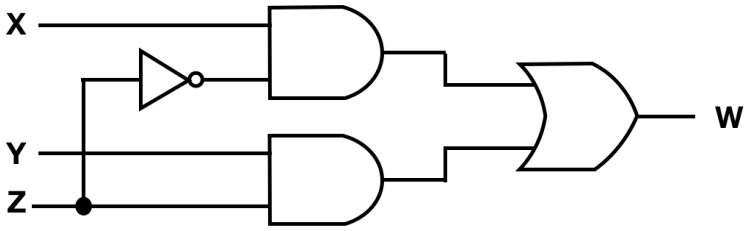
B. (Draw the circuit only) Find a minimum multiple-level gate implementation using AND gates, OR gates, and inverters.

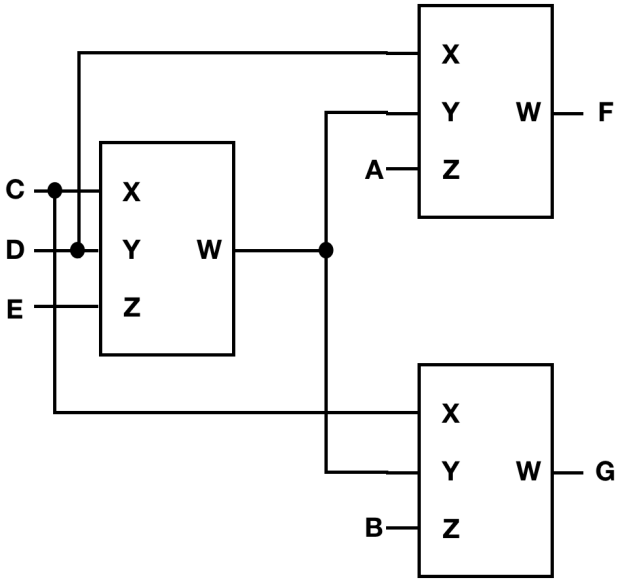


4. (Draw the circuit only) Design a circuit to implement the following pair of Boolean equations:

$$F = A(C\overline{E} + DE) + \overline{A}D$$
$$G = B(C\overline{E} + DE) + \overline{B}C$$

To simplify drawing the schematic, the circuit is to use a hierarchy based on the factoring shown in the equation. Three instances (copies) of a single hierarchical circuit component made up of two AND gates, an OR gate, and an inverter are to be used. Draw the logic diagram for the hierarchical component and for the overall circuit diagram using a symbol for the hierarchical component.





5. (Draw the circuit only) A hierarchical component with the function $H = \overline{X}Y + XZ$ is to be used along with inverters to implement the following equation:

$$G = \overline{A}\,\overline{B}C + \overline{A}BD + A\overline{B}\,\overline{C} + AB\overline{D}$$

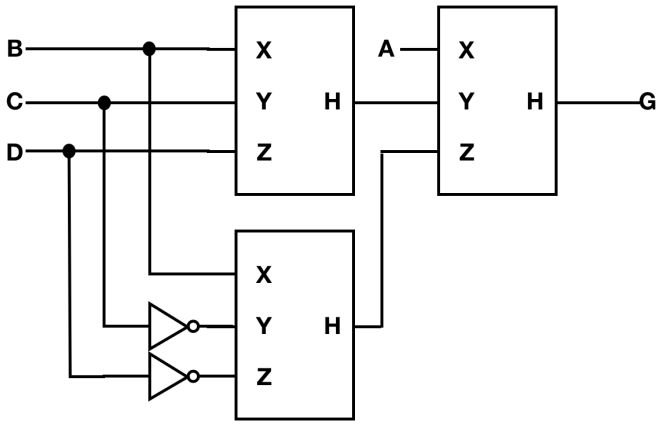
The overall circuit can be obtained by using Shannon's expansion theorem,

$$F = \overline{X} \cdot F_0(X) + X \cdot F_1(X)$$

where $F_0(X)$ is F evaluated with variable $X = 0$ and $F_1(X)$ is F evaluated with variable $X = 1$. This expansion F can be implemented with function H by letting $Y = F_0$ and $Z = F_1$. The expansion theorem can then be applied to each of F_0 and F_1 using a variable in each, preferably one that appears in both true and complemented form. The process can then be repeated until all F_i's are single literals or constants. For G, use $X = A$ to find G_0 and G_1 and then use $X = B$ for G_0 and G_1. Draw the top-level diagram for G using H as a hierarchical component.

$$H(X, Y, Z) = \overline{X}Y + XZ$$

$$\begin{aligned} G &= \overline{A}H(B, C, D) + AH(B, \overline{C}, \overline{D}) \\ &= H(A, H(B, C, D), H(B, \overline{C}, \overline{D})) \end{aligned}$$



6. (Draw the circuit only) Design a 16-to-1 multiplexer using 4-to-16 decoder and a 16 2-input AND gate and a 16-input OR gate.

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