04.02.20 14:27

CSCI 150
Introduction to Digital and Computer System Design
Lecture 2: Combinational Logical Circuits V

Jetic Gū

2020 Winter Semester (S1)

P0
XXXXXXX

2 Types of Knowledge

Nothing

P0
XXXXXXX

2 Types of Knowledge

1. I know this by heart!
   - Important Definitions, Number Systems and Arithmetics, Boolean Algebra
2. Whatever, I can look it up when I need it.
   - The rest of lecture 2 today.
   - You need to know where to look at if you don’t remember later!

Nothing

Overview

- Focus: Boolean Algebra
- Architecture: Combinatory Logical Circuits
- Textbook v4: Ch2 2.8, 2.9. 2.10; v5: Ch2 2.6, 2.7
- Core Ideas:

    1. Other Gate Types: XOR, NAND, NOR, Buffer, High-Impedance, Odd Function

    2. Lecture 2 Review

P0
Review

Boolean Algebra I-III

I. AND, OR, NOT Operators and Gates

- Simple digital circuit implementation
- Algebraic manipulation using Binary Identities

II. Standard Forms

- Minterm & Maxterm
- Sum of Products & Product of Sums

III. Optimisation Using K-Map (For 2,3,4 Variables)

Review

Other Gate Types

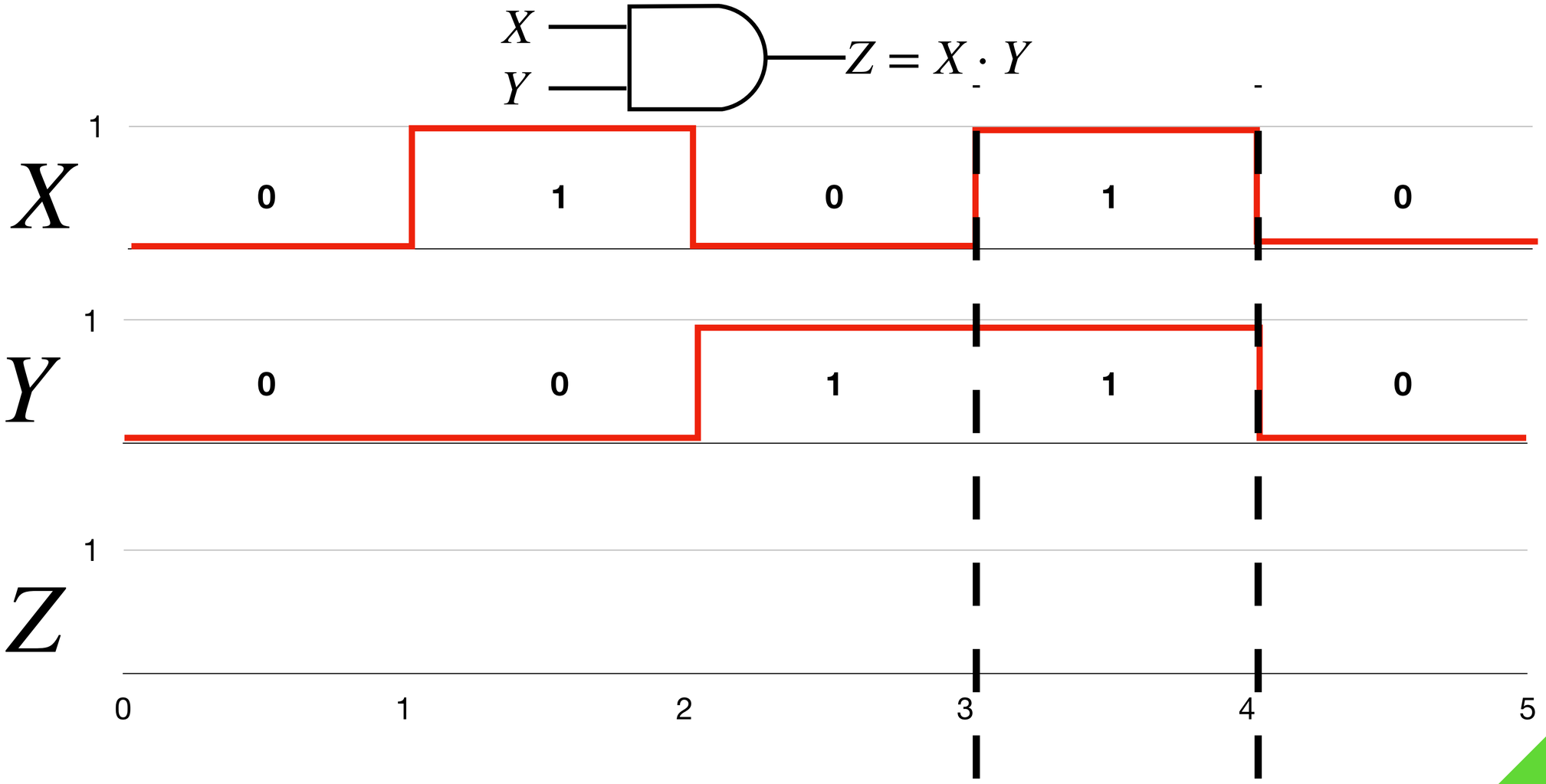
Delay Propagation
XOR, NAND, NOR, Buffer

Summary

P1
Other Gates

Gate Delay

Timing Diagram (**REALITY**)

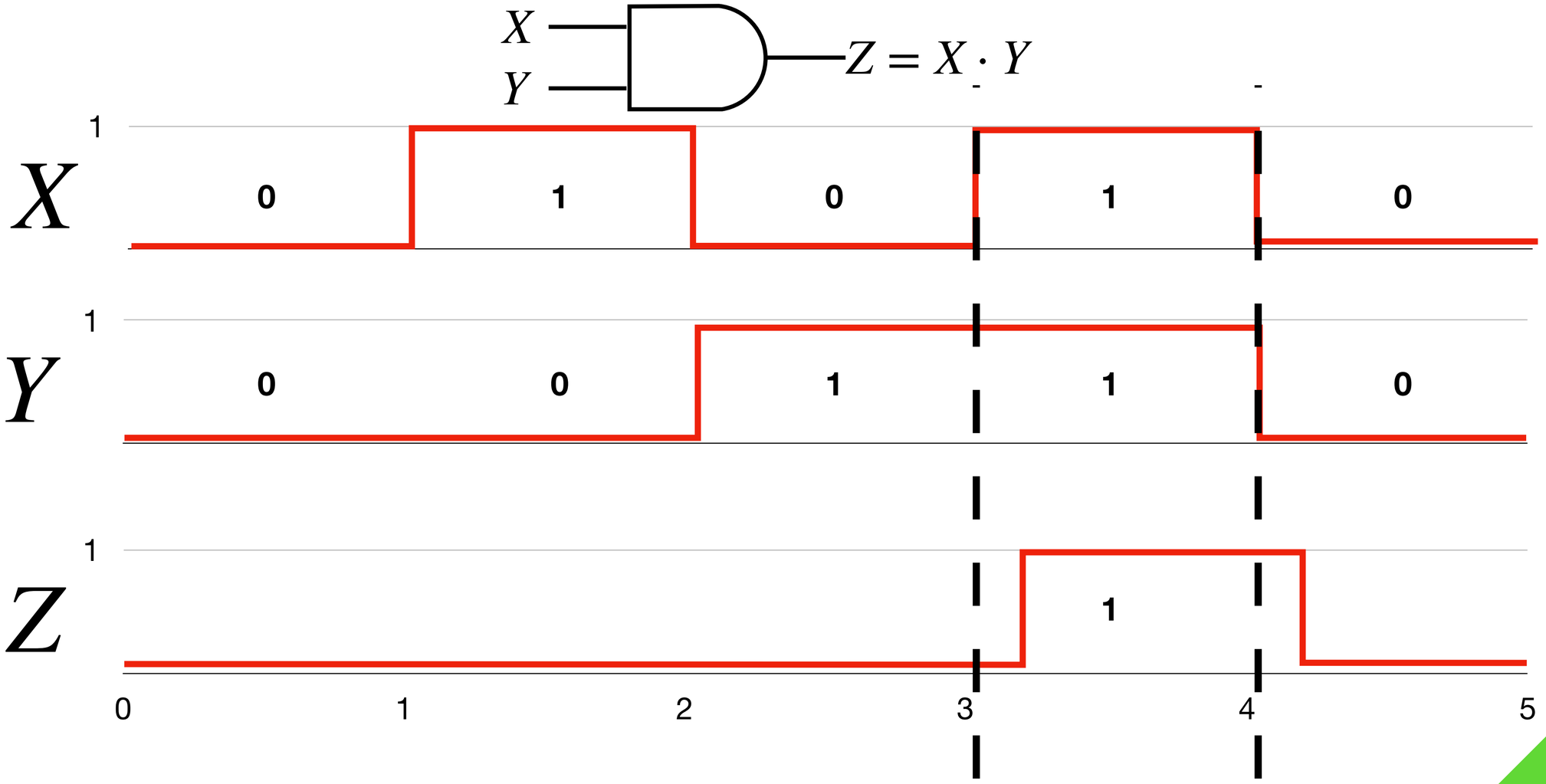


Review

P1
Other Gates

Gate Delay

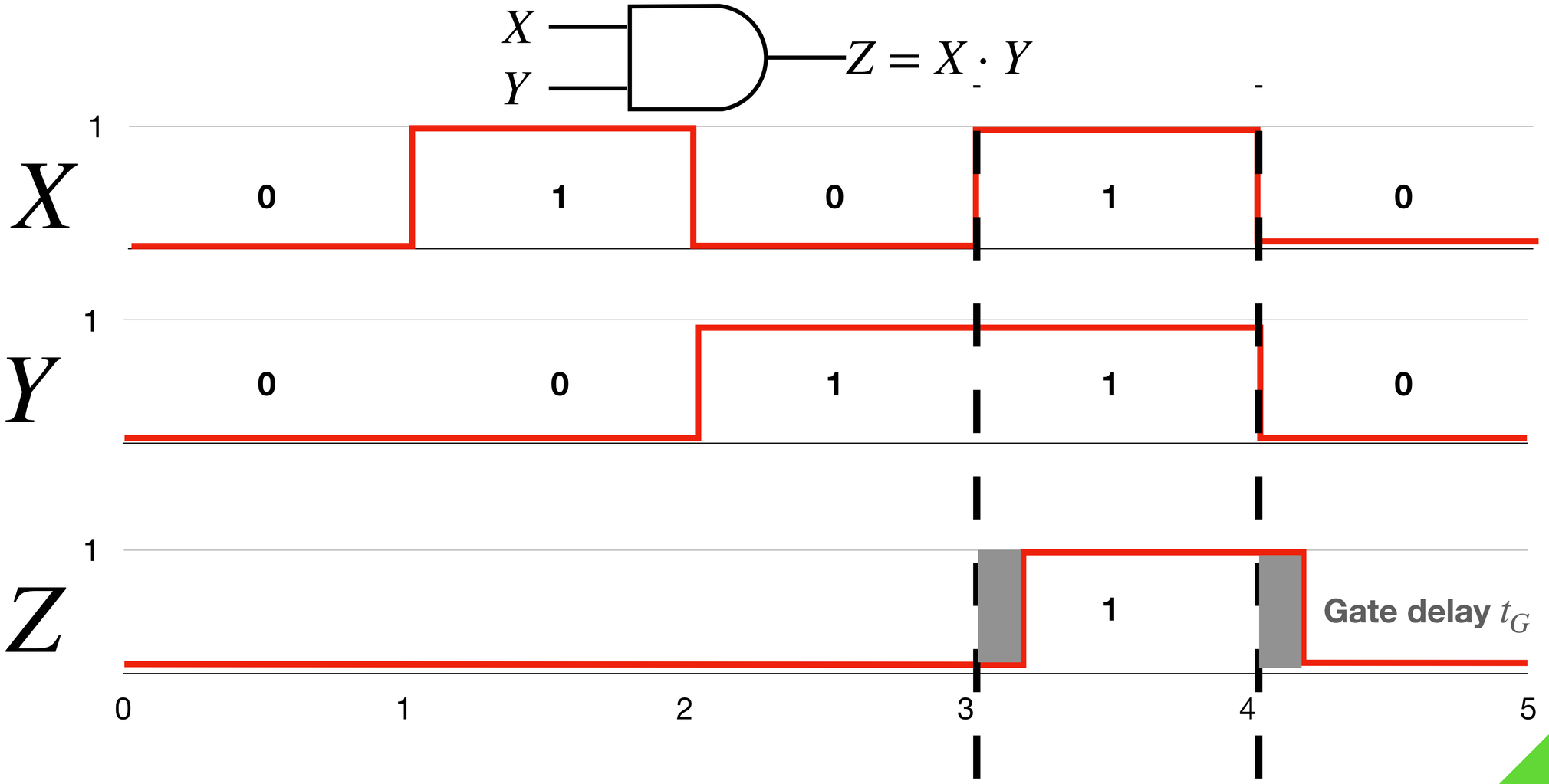
Timing Diagram (**REALITY**)



Review

Gate Delay

Timing Diagram (REALITY)



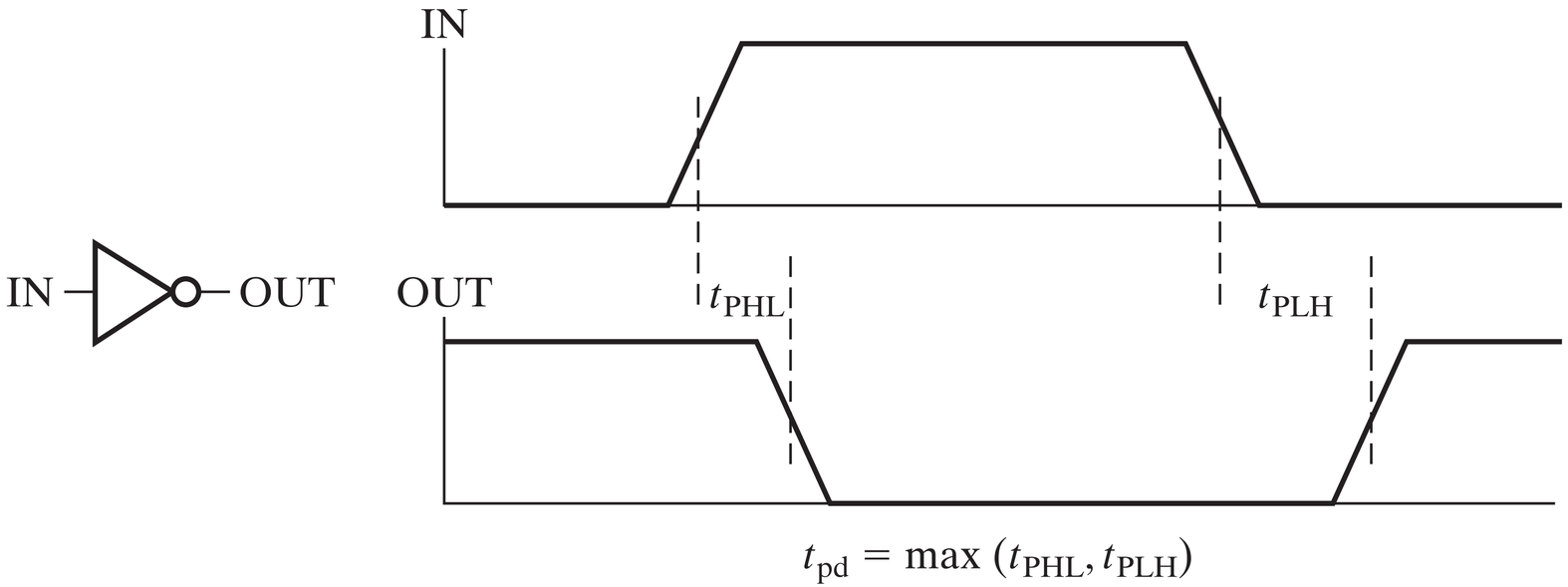
Review

Delays

- Gate Delay
  - The time required for a change in value of a signal to propagate from input to output (of a Gate)
- Propagation Delay
  - The time required for a change in value of a signal to propagate from input to output (of a Circuit)

Concept

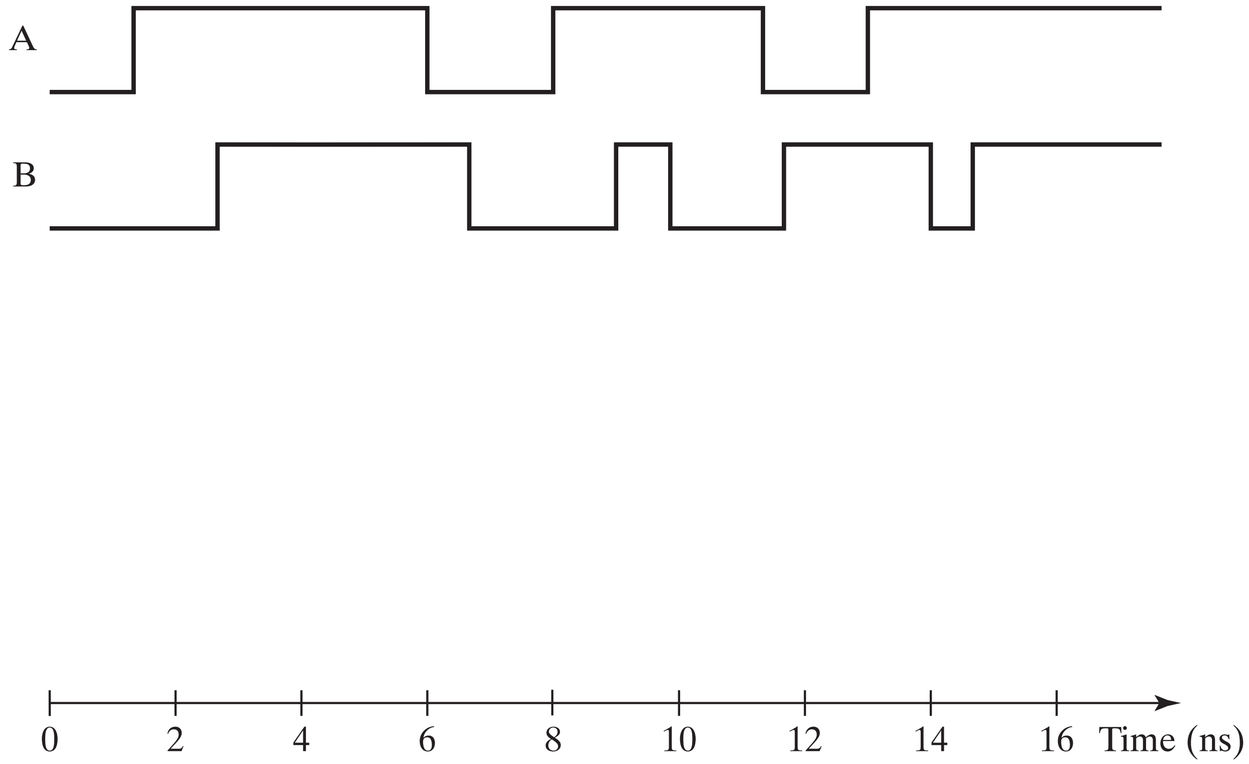
Delays



- t_{pd}: Propagation Delay: longest time for propagating from input to output
  - t_{PHL}: Hight2Low propagation time; t_{PLH}: Low2High propagation time;

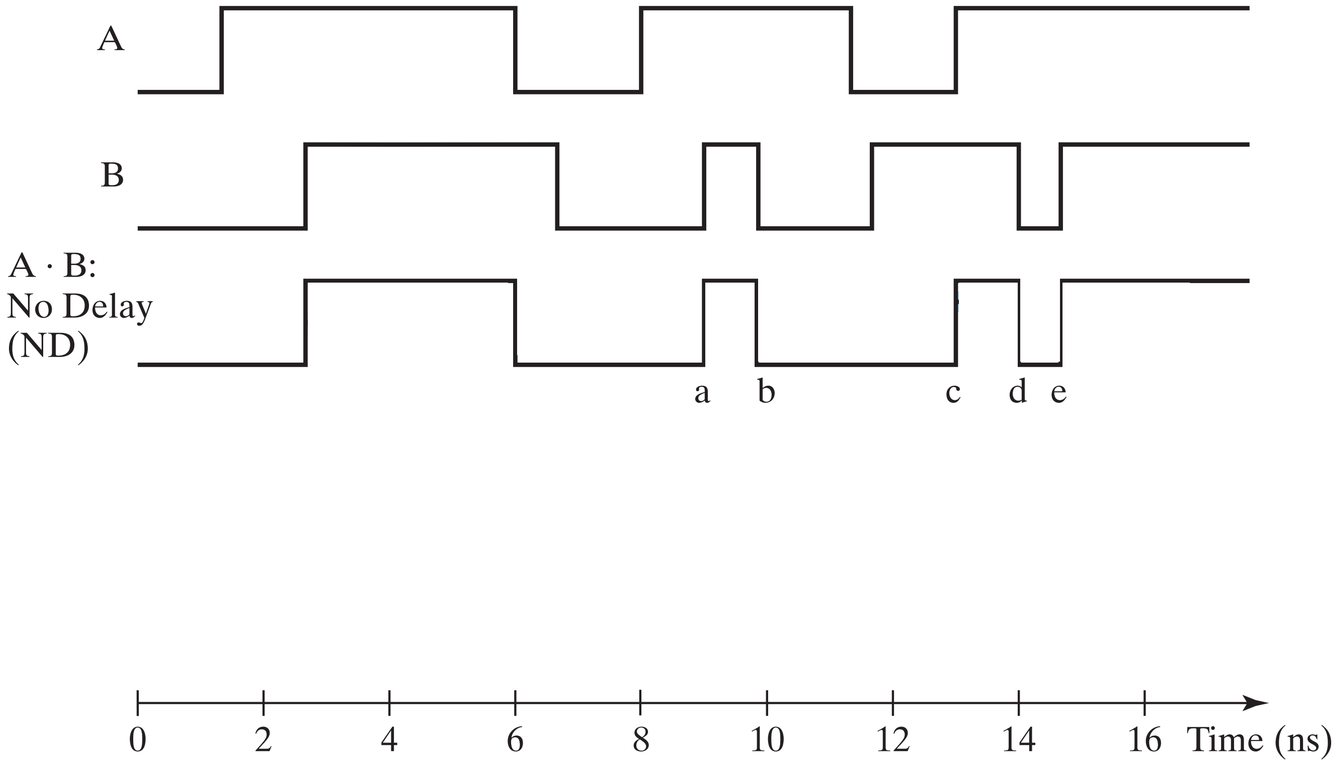
Concept

Transport and Inertial Delays



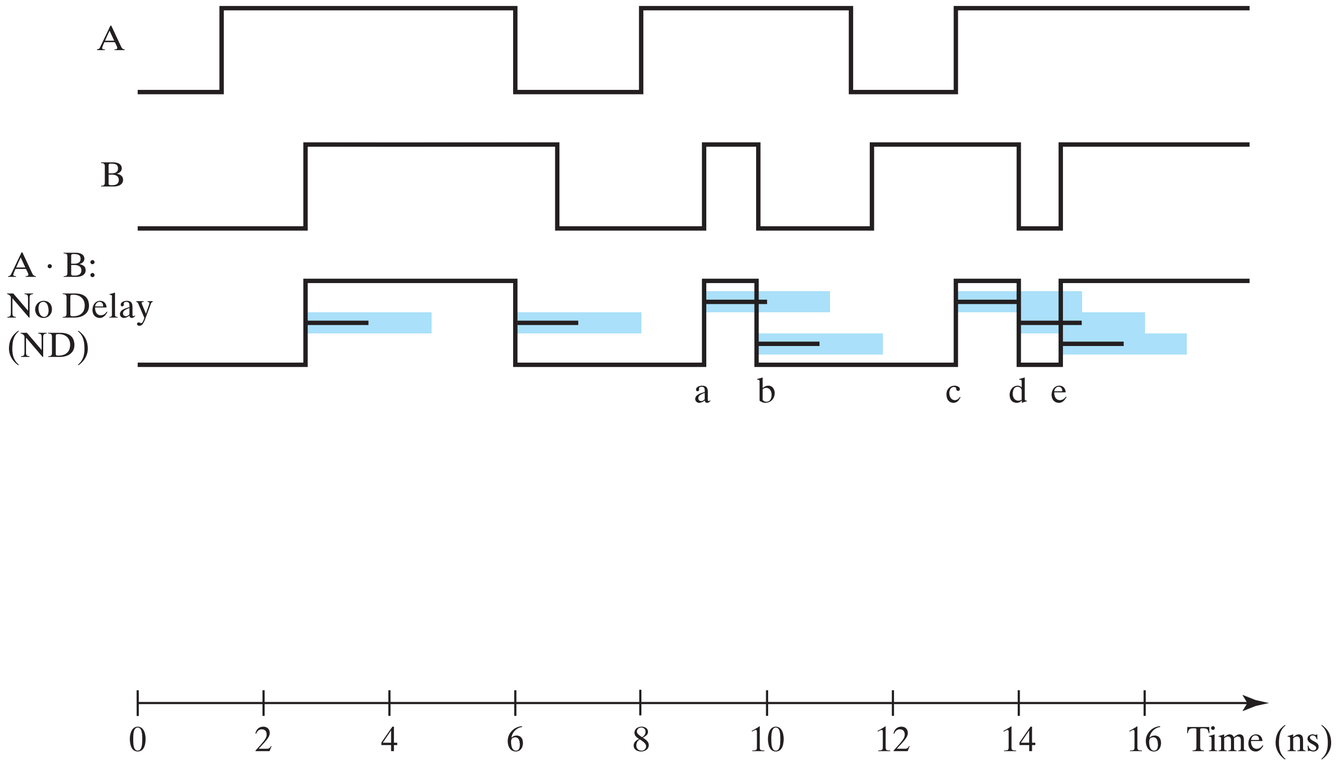
Concept

Transport and Inertial Delays



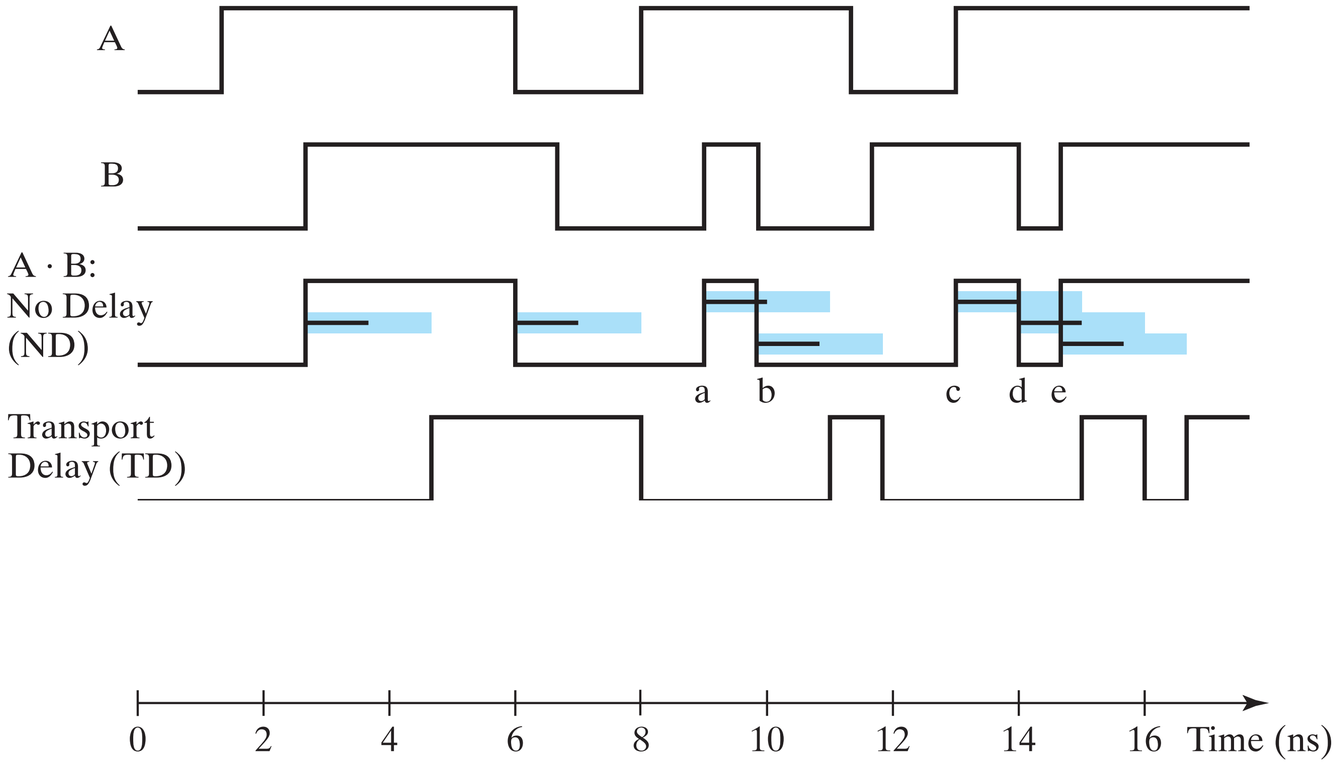
Concept

Transport and Inertial Delays



Concept

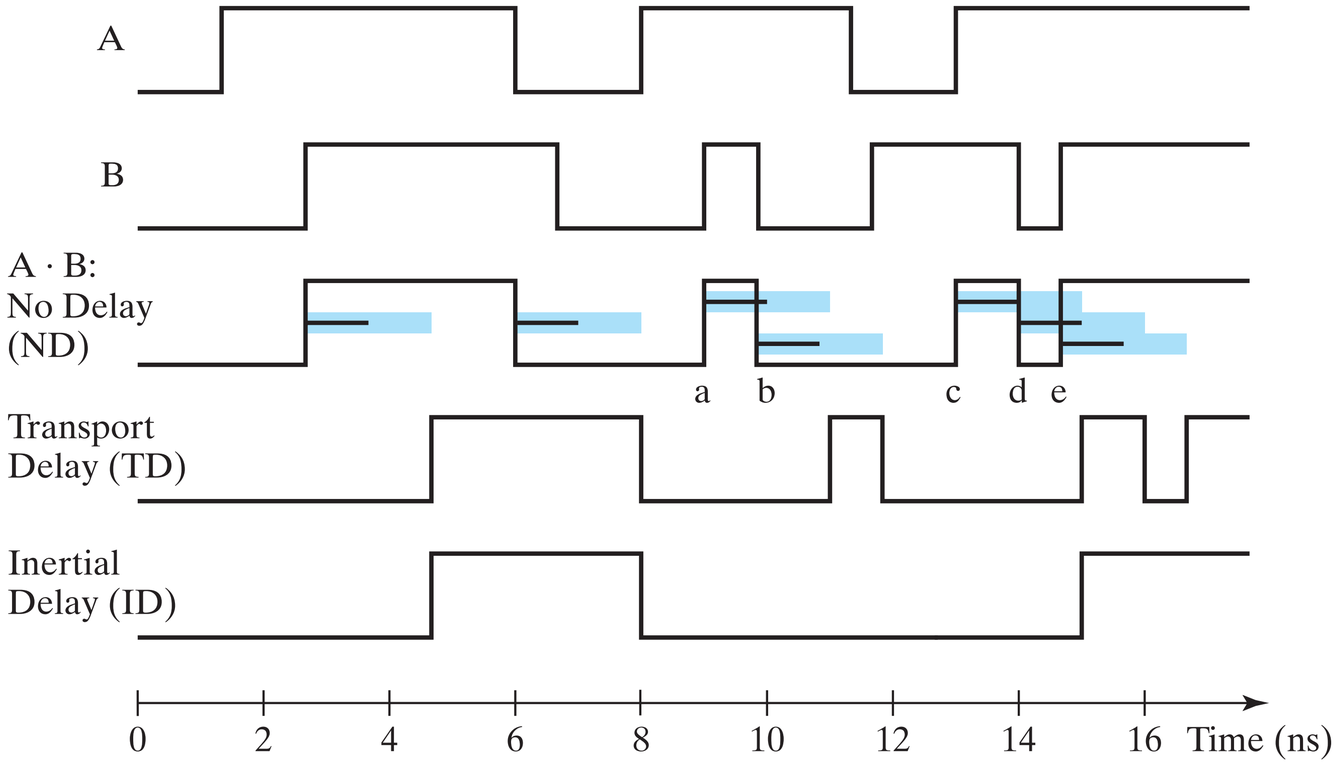
Transport and Inertial Delays



- **Transport Delay**: output in response to input changes after propagation delay

Concept

Transport and Inertial Delays



- **Transport Delay**: output in response to input changes after propagation delay
- **Inertial Delay**: if a value changes twice in a short time (**rejection time**), ignore

Concept

Parameters of Gate Delay

Concept

Parameters of Gate Delay

- Fan-in
  number of inputs of a logic gate

Parameters of Gate Delay

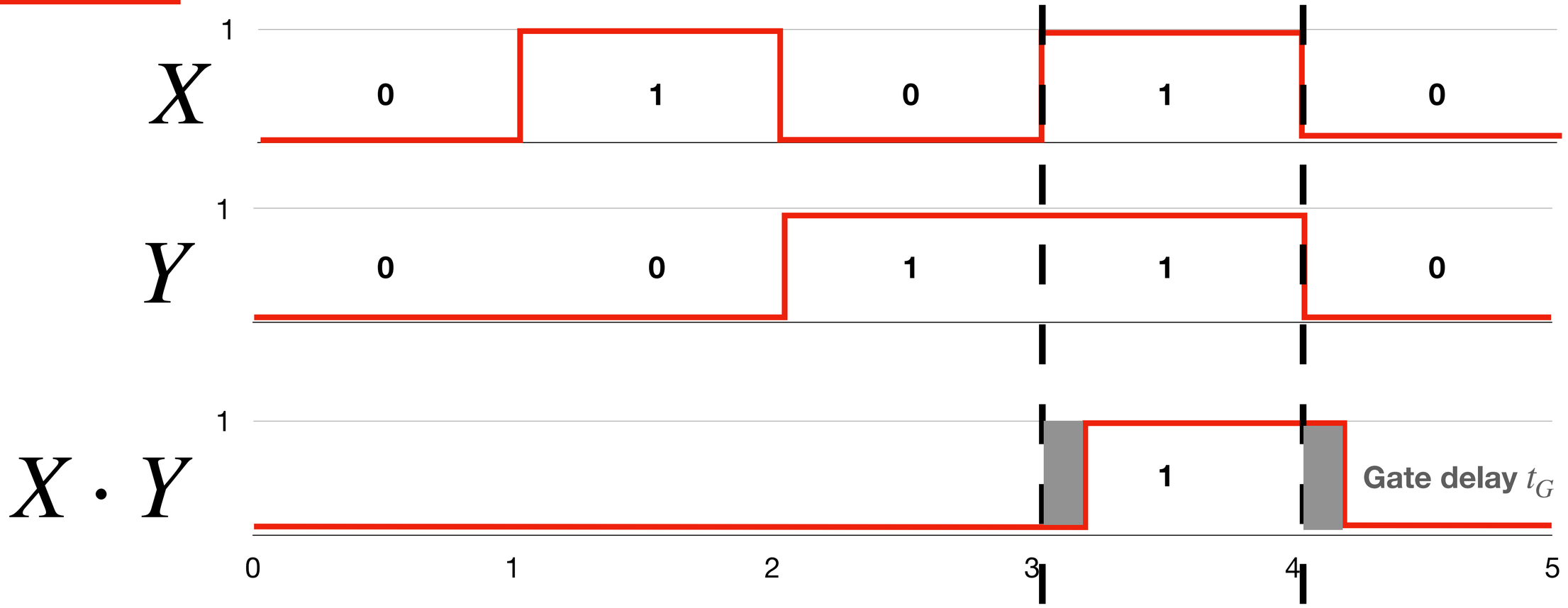
- Fan-in
  number of inputs of a logic gate

- Fan-out (standard load)
  number of gates that each logic gate can drive while providing voltage levels in the guaranteed range is called the standard load or fan-out

Concept

P1
Other Gates

Standard Load

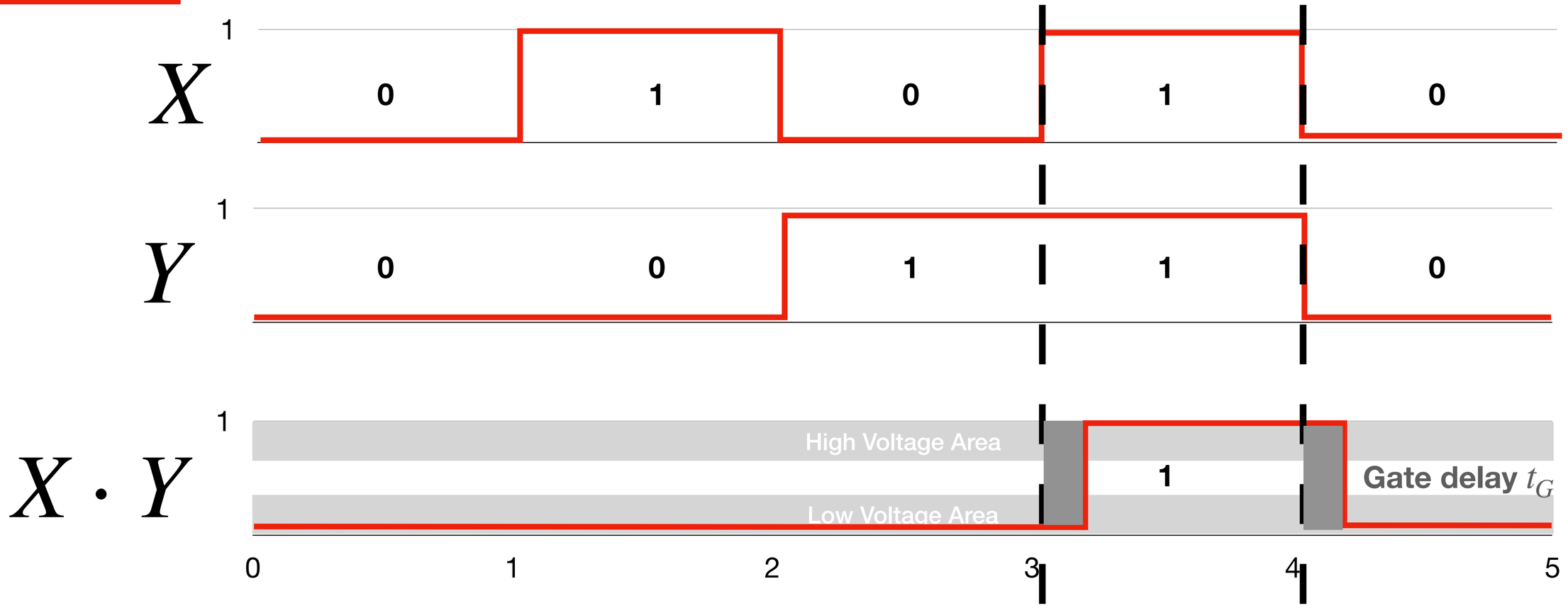


- Digital circuits are driven by power, each component also takes power

Demo

P1
Other Gates

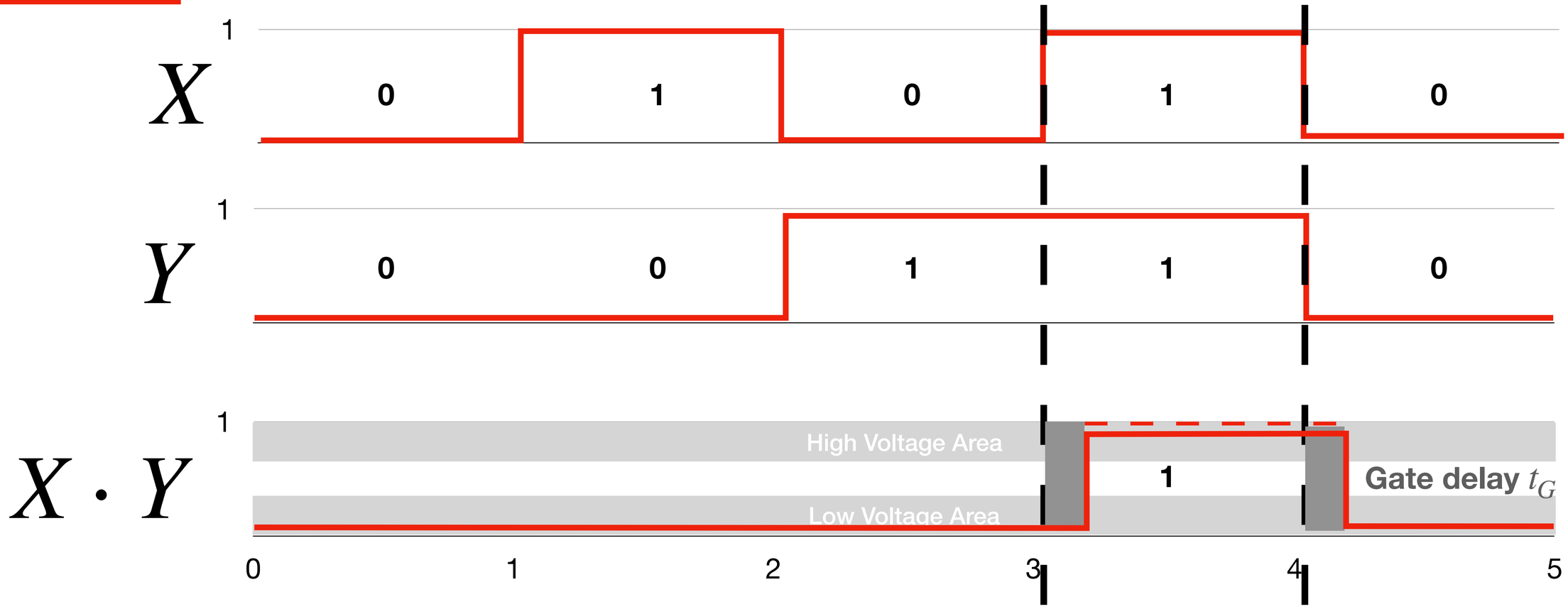
Standard Load



- Digital circuits are driven by power, each component also takes power

Demo

Standard Load



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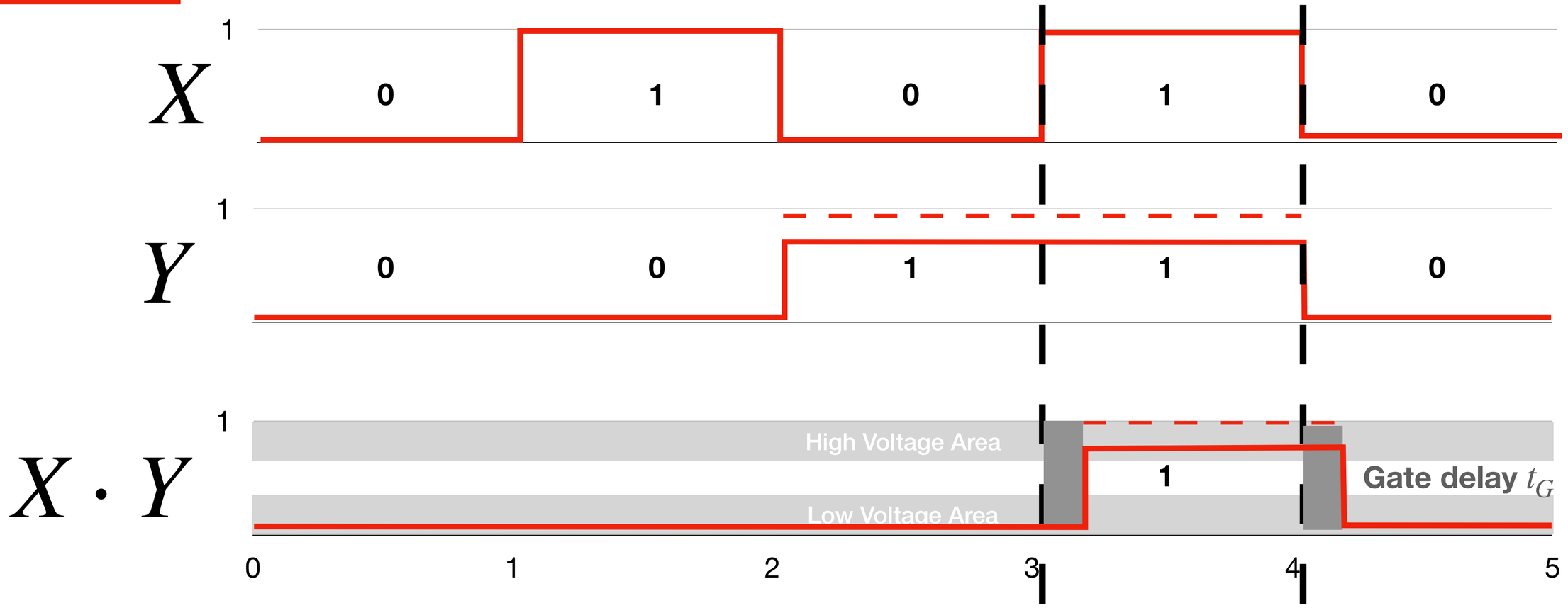
Demo

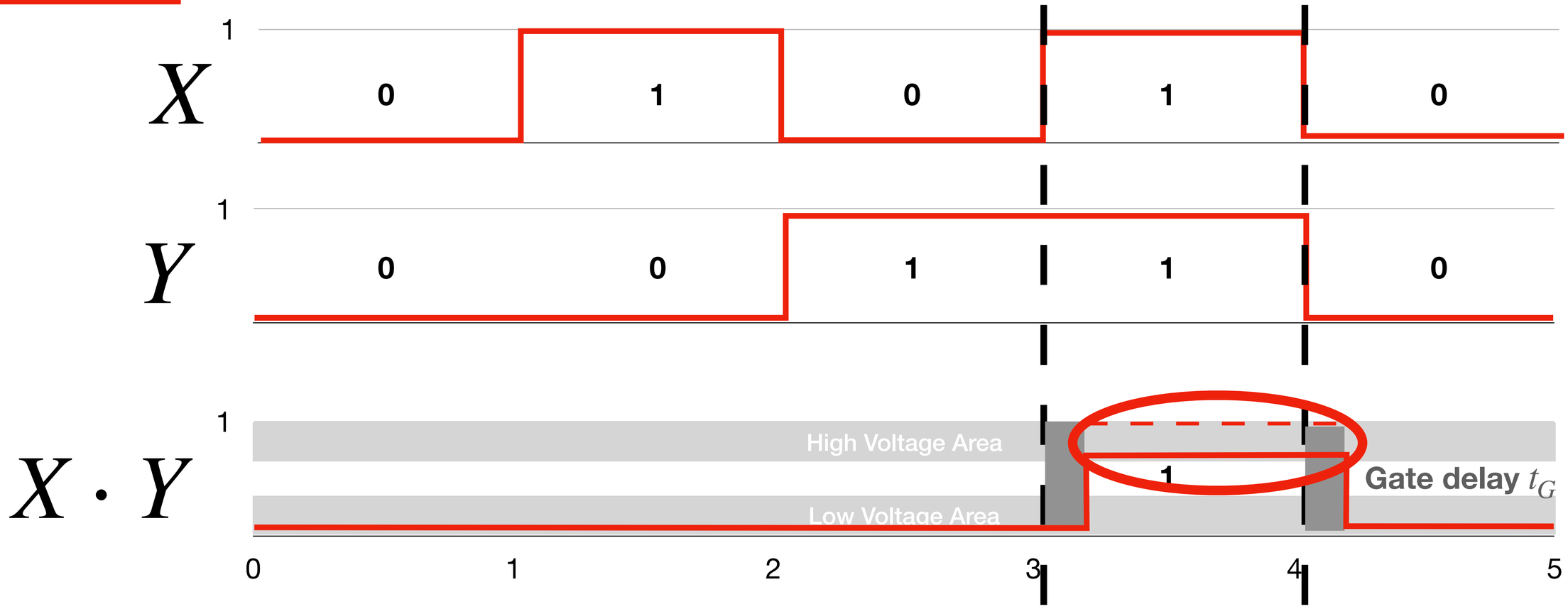
Standard Load



- Changes in input voltage can also affect output voltage

Demo

Standard Load

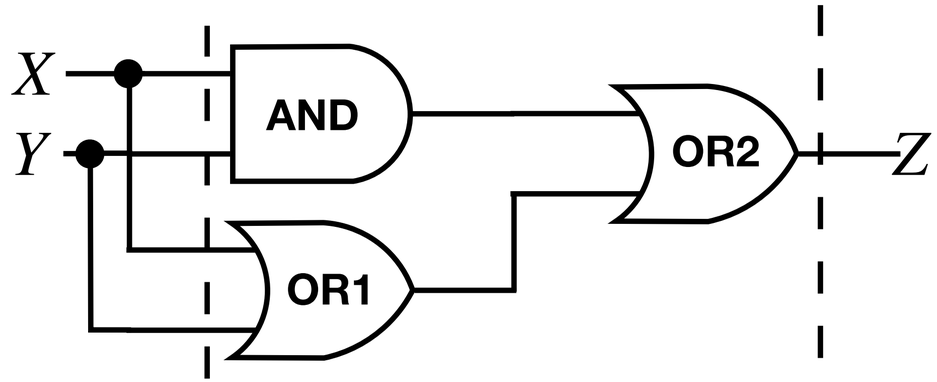


- If it takes too much power, it will not be able to guarantee output voltage
- Standard load is defining that power consumption, which also affect delay

Demo

P1
Other Gates

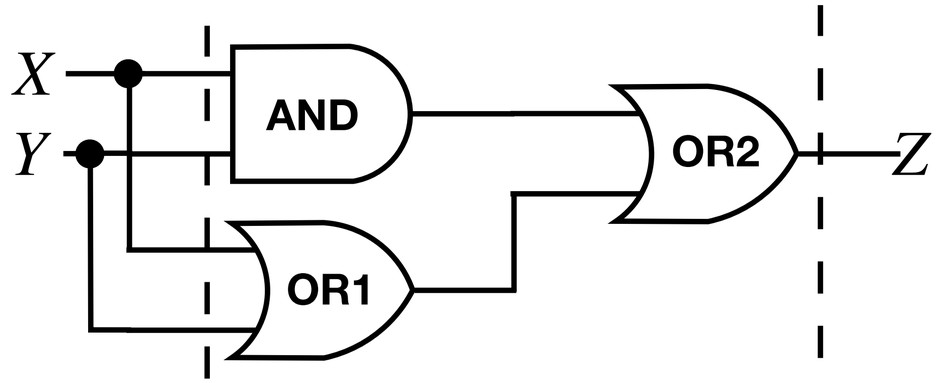
Standard Load



- OR Gate: 0.8 SL; AND Gate: 1.00 SL;
- Delay for AND:
  $t_{pd} = 0.07 + 0.021 \times \sum InputSL$
- Delay for OR:
  $t_{pd} = 0.05 + 0.02 \times \sum InputSL$

Demo

Standard Load

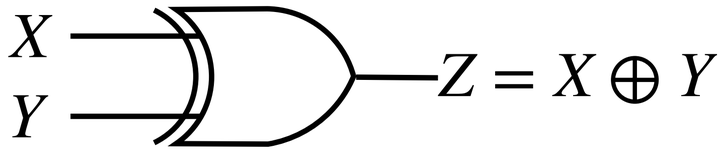


- OR Gate: 0.8 SL; AND Gate: 1.00 SL;
- Delay for AND:
  $t_{pd} = 0.07 + 0.021 \times \sum InputSL$
- Delay for OR:
  $t_{pd} = 0.05 + 0.02 \times \sum InputSL$
- Estimation for OR2
  $t_{pd} = 0.05 + 0.02 \times (0.8 + 1.00) = 0.086\text{ns}$
- Precise estimation is very hard, since we lack a lot of these information
- We can ignore this computation, but you should know roughly

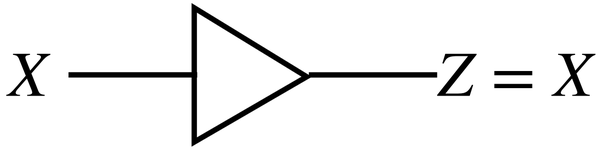
Demo

Other Gates

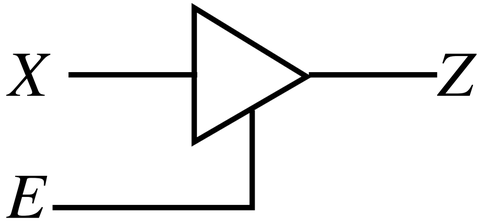
XOR Gate
Exclusive-OR



Buffer



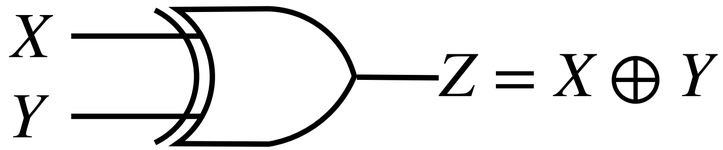
3-State Buffer



Concept

Buffer

XOR Gate
Exclusive-OR



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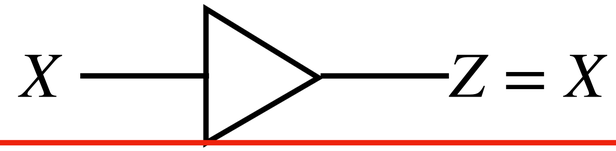

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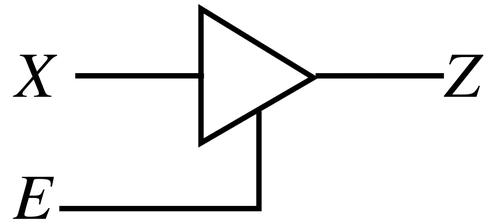
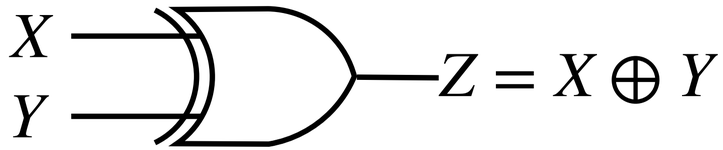


- Has delay
- Increases output Voltage
  e.g.: input 0.8 V, output 1.0 V

Concept

3-State Buffer

XOR Gate
Exclusive-OR



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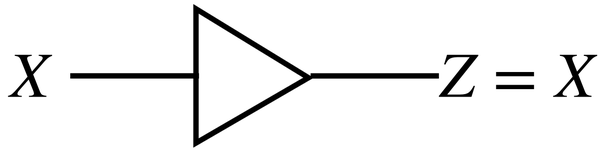

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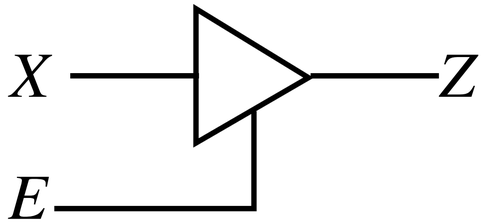

- Has delay
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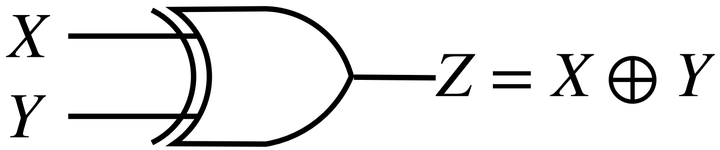
- When $E = 0$, outputs no electricity
  (Open circuit/Hi-Z/High Impedance)

Concept

3-State Buffer

XOR Gate
Exclusive-OR



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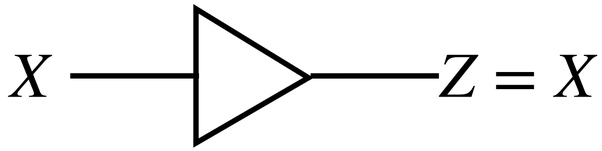

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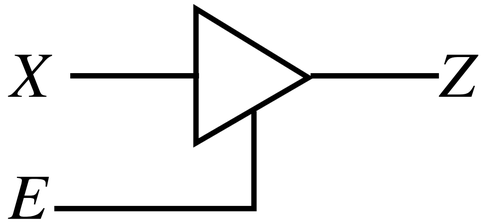

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Concept

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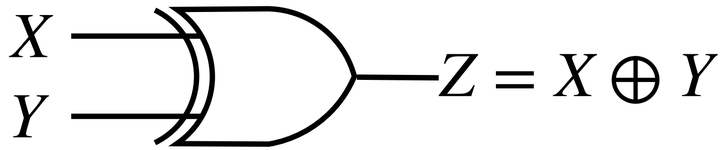

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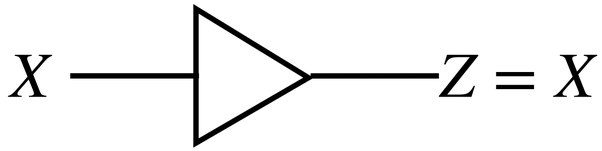

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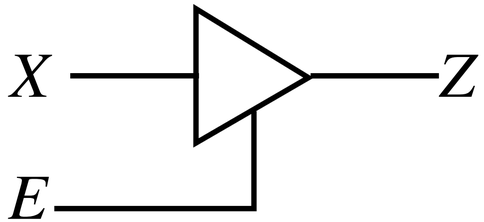

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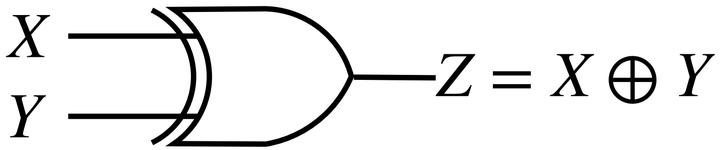

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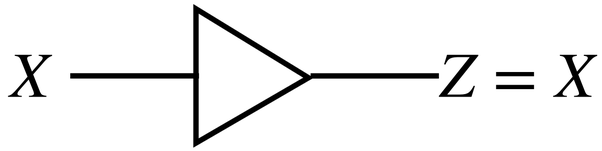

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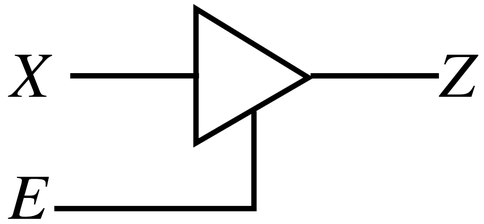


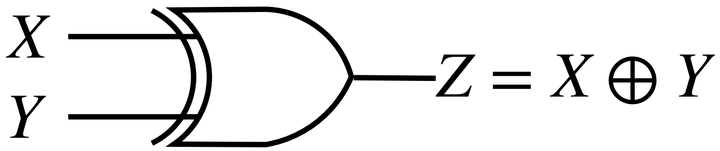
3-State Buffer Truth Table

E	X	Z
0	0	Hi-Z
0	1	Hi-Z
1	0	0
1	1	1

Concept

XOR Gate

XOR Gate
Exclusive-OR



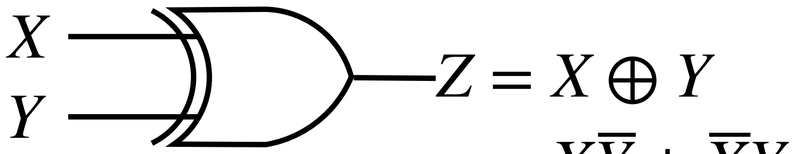
XOR Truth Table

X	Y	$Z = X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0

Concept

XOR Gate

XOR Gate
Exclusive-OR



$$Z = X \oplus Y$$
$$= X\overline{Y} + \overline{X}Y$$

XOR Truth Table

X	Y	$Z = X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0

Concept

XOR Gate

- $X \oplus 0 = X$
- $X \oplus X = X$
- $X \oplus \overline{Y} = \overline{X \oplus Y}$
- $X \oplus 1 = \overline{X}$
- $X \oplus \overline{X} = 1$
- $\overline{X} \oplus Y = \overline{X \oplus Y}$

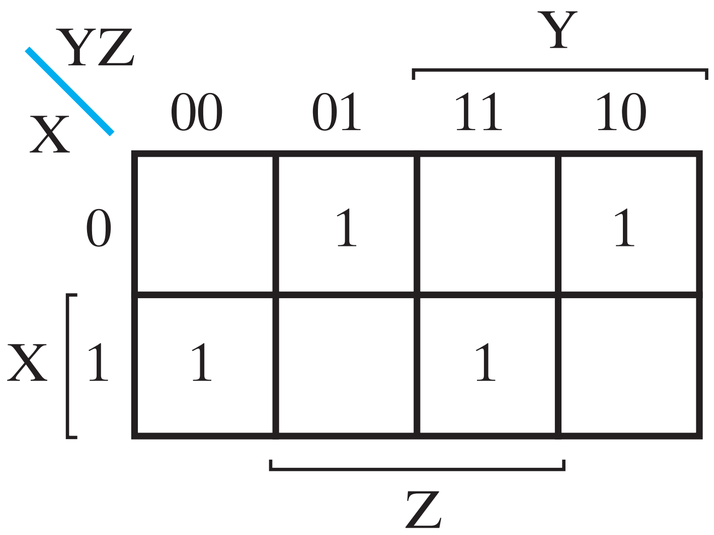
Concept

Odd and Even Functions

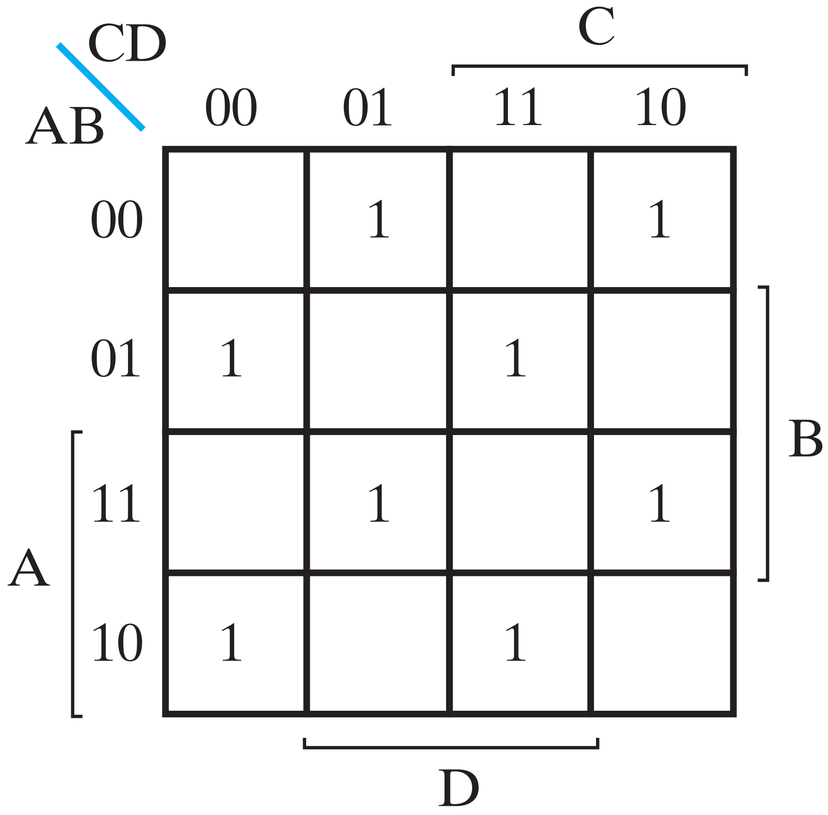
- Odd Functions
  - Outputs 1 if the **number of 1s** in the input is an **Odd** number
  - 2 variables: XOR
- Even Functions
  - Outputs 1 if the **number of 1s** in the input is an **Even** number
  - 2 variables: XNOR

Concept

Odd Function K-Map



(a) $X \oplus Y \oplus Z$

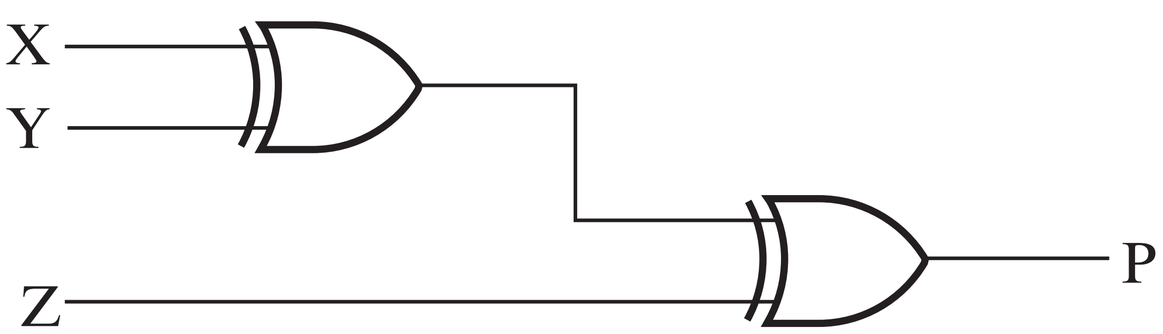


(b) $A \oplus B \oplus C \oplus D$

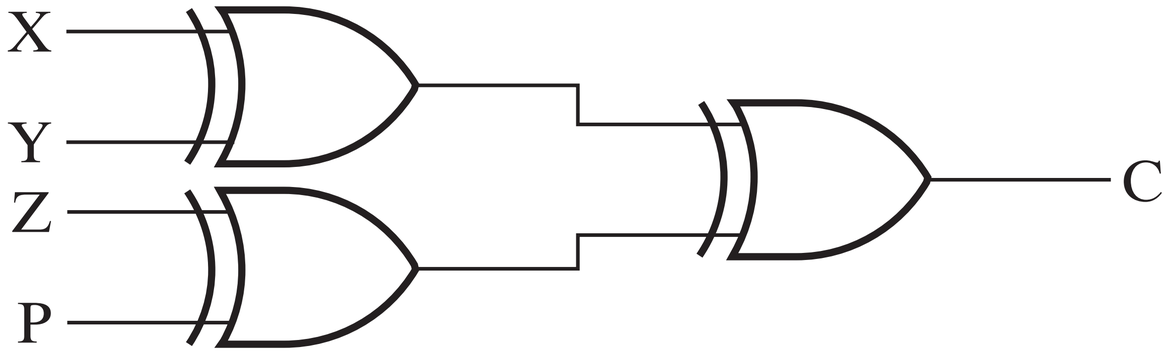
Concept

P1
Other Gates

Odd Function Boolean Expressions



(a) $P = X \oplus Y \oplus Z$

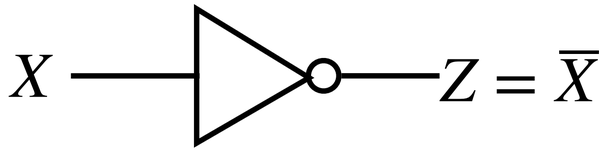


(b) $C = X \oplus Y \oplus Z \oplus P$

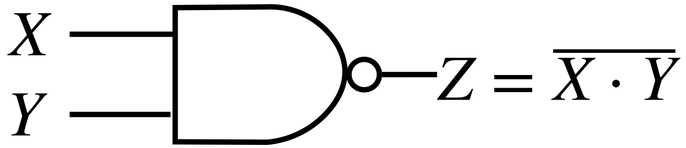
Concept

N-Gates

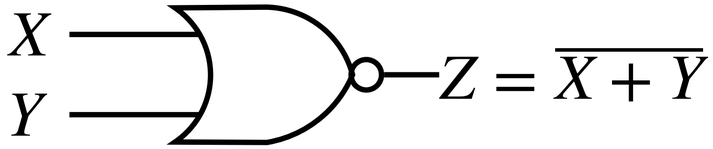
NOT Gate



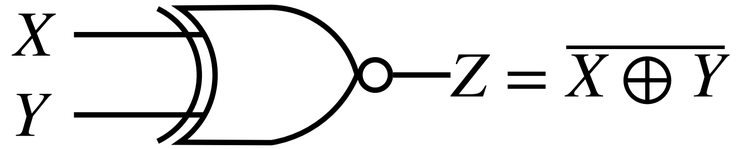
NAND Gate



NOR Gate



XNOR Gate



P1
Other Gates

Summary

Review

Summary

- Delay: Remember the Definitions!

Review

Summary

- Delay: Remember the Definitions!
  - Gate Delay and Propagation Delay

Review

Summary

- Delay: Remember the Definitions!
  - Gate Delay and Propagation Delay
  - Transport and Inertial Delays

Review

Summary

- Delay: Remember the Definitions!
  - Gate Delay and Propagation Delay
  - Transport and Inertial Delays
  - Standard Load

Review

Summary

- Delay: Remember the Definitions!
  - Gate Delay and Propagation Delay
  - Transport and Inertial Delays
  - Standard Load
- Other Gates: Remember the Definitions!

Review

Summary

- Delay: Remember the Definitions!
  - Gate Delay and Propagation Delay
  - Transport and Inertial Delays
  - Standard Load
- Other Gates: Remember the Definitions!
  - XOR, Buffer, 3-State, NAND, NOR

Review