### CSCI 150 Introduction to Digital and Computer System Design Lecture 2: Combinational Logical Circuits I



Jetic Gū 2020 Winter Semester (S1)



### Overview

- Focus: Boolean Algebra
- Architecture: Combinatory Logical Circuits
- Textbook v4: Ch2 2.1 2.2; v5: Ch2 2.1 2.2
- Core Ideas:
  - Logical Gates 1.
  - 2. Introduction to LogicWorks

### Logic Gates And, Or, Not Gates, LogicWorks



- A basic circuit unit implemented using transistors and interconnections
  - gate, but only it's external properties
  - Performs a single logical operation

# What is a Logic Gate?

• We when analysing a digital circuit, are not concerned with the internals of a

operate on one or more binary input signals to produce an output signal



- Similar to in electric circuit design, we are not concerned with the design of the lightbulb or battery, but we know what it does.
- A logic gate is like that, we know it's external logic properties, that's enough.

# What is a Logic Gate?







**AND Gate** 

**OR Gate** 

**NOT Gate** 

## First 3 Gates



### AND Operator and Boolean Algebra / Binary Logic



- Boolean Algebra
  - Each variable can only have one of two values:
    - TRUE/ON/1
    - False/OFF/0
- AND: Z is equal to X AND Y
  - Operator: · (\cdot)



### AND Operator and Boolean Algebra



- AND: Z is equal to X AND Y
  - Operator: · (\cdot)
- Truth Table
  - Left: all combinations of input values
  - Right: corresponding output values







OR Truth Table

X	Y	Z = X + Y
0	0	0
0	1	1
	0	1
1	1	1

### **OR Operator**

- OR: Z is equal to X or Y
  - Operator: +







### NOT Operator

- NOT: Z is equal to NOT X
  - Operator:  $\overline{X}$  (\overline{X})
  - Also called: *Complement* operation; *Inverter* gate



### Logic Gate and Boolean Algebra

- Logic Gates
  - AND Gate, OR Gate, NOT Gate
  - Actual physical components

### THEY HAVE DIFFERENCES!

- Boolean Algebra Operators
  - AND (·), OR (+), NOT  $(\overline{X})$
  - Mathematical Representations



# **Digital Logical Gates**

- In math, everything happens simultaneously
  - An equation like 250 + 760 = 1010 doesn't change with time/location
- In digital circuits, we have electrons as 'messengers'. They travel at about 2,200 kilometres per second
  - Logic gates are tiny circuits, which means they still have internal components: even slower
  - This means: there will be tiny delays called Gate Delay





0	1	0

1 1	0
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## Gate Delay

- Gate delay are small, but not ignorable in practice
  - for simulation, you can ignore it for now
- Gate delay differs for different types and implementations of Gates





## Simulation 1

### Truth Table

X	Y	$Z = (X \cdot Y) + (X + Y)$
0	0	
0	1	
1	0	
1	1	





## Simulation 2







## Simulation 3











# Summary

- AND, OR, NOT Operators
- Logic Gates
- Timing diagram
- Truth Table
- Gate Delay





### LogicWorks Fire up your computer please!





Welcome to LogicWorks		×	
	Create a new, empty circuit Create a new circuit diagram	Create	
	Open an Example File Open one of the example files provided with LogicWorks.	Examples	
Open an Existing Design C:\Program FilescWorks S	5\Examples\Simulate.CCT	Open Browse	
Create a Simulation Model Use the Model Wizard to define a new simulation model using either VHDL or a circuit diagram.			
Continue with No Circuit Open		Cancel	





### 1. This is the main interface





### 1. Select Simulation IO from the Parts Palette



### 1. Pay Attention to Binary Probe and Binary Switch



LogicWorks 5 - [Circuit1.cct] 😤 File Edit View Schematic Simulation Window Help D ☞ 🖬 🚳 🔏 🖿 🕄 ₽ 🔍 🔊 🔍 🔉 + + 🛎 💶 💷 🕸 👬 🭕 독 뜻 🖉 🔐 값 🛠 🗣 💺 🗢 🗙 = 😐 እ 🖍 0 ns -94 Z < ₽ Circuit 1.cct 200 400 ns < Timing /

1. Double click and place one of each on the main board

Ready

**P2** 

**Tutorial** 







1. Use the 'Draw Signal' tool to connect the two parts





1. Switch back to the Cursor mode, now click on the switch and you can change the signal value



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1. Select Simulation Gates



1. Select AND-2, then complete the above diagram



1. Select Clock from Simulation IO, then replace the lower Binary Switch with it. A Clock is a device that generates a 1 at a certain frequency



1. Select Clock from Simulation IO, then replace the lower Binary Switch with it



1. Right click the **Red Wire**, select **Name** 





1. Complete the diagram like above, then click Reset Simulation





1. Use the Simulation Panel to control the speed of simulation, then you will see the Timing Diagram!





- Curtain Motor Control
  - Button1: 1 when user wants to open the curtain
  - Button2: 1 when user wants to close the curtain
  - Output1: 1 to make the motor open the window
  - Output2: 1 to make the motor close the window
  - Light: motor is active

### Exe 1



• When both buttons are pressed, motors do nothing







- Curtain Motor Control
  - Sensor1: 1 when curtain is fully closed
  - Sensor2: 1 when curtain is fully open
  - Button1: 1 when user wants to open the curtain
  - Button2: 1 when user wants to close the curtain
  - Output1: 1 to make the motor open the window
  - Output2: 1 to make the motor close the window
  - Light: motor is active

### Exe 2



• Stop the motor when the curtain is already fully opened/ closed





# Summary

- Simulation in LogicWorks
- Binary Probe / Binary Switch in LogicWorks
- Gates in LogicWorks
- Clocks in LogicWorks
- Timing Diagram in LogicWorks

