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1. Handwritten submissions and proprietary formats (e.g. Pages or MS Word) **will not be graded**.
2. Late submission and resubmission policies are stated on the course webpage.
3. Circuits must be **tested**. Untested circuits will receive 0.

Submission File structure:

```
submission.zip
    — answer.pdf
    — c1-1.cct
    — c1-2.cct
    — c2.cct
    — c3.cct
```

The files `circuit1-1`, `circuit1-2`, `circuit2` 2pt each, `circuit3` 4pt, `answer.pdf` 2pt.

Lab 7

1. (PDF) Datapath conceptual question: assume a datapath with a 4-bit register array (4 GPRs inside) that can perform certain functions. The datapath takes input $OP_{2:0}$ from the control unit for function selection, $rd_{1:0}$ and $rs_{1:0}$ for register selection, $in_{3:0}$ for value input.

$OP_{2:0}$	**Register Operation**
000	No change
001	Clear a single register to 0, selected by $rd_{1:0}$
010	Perform register transferring, assign the value of register at address $rs_{1:0}$ to register at $rd_{1:0}$.
011	Load value from $in_{3:0}$ into a single register, selected by $rd_{1:0}$
110	Perform addition of 2 register values, selected by $rd_{1:0}$ and $rs_{1:0}$, store the output to register with address $rd_{1:0}$. (Use the adder-subtractor functional block)
111	Perform subtraction of 2 register values, selected by $rd_{1:0}$ and $rs_{1:0}$, store the output to register with address $rd_{1:0}$. (Use the adder-subtractor functional block)

Write down the sequence for all necessary inputs for computing 4 + 5 - 7. You will need to load number 4, 5, 7 into the datapath, then perform the necessary calculation, and finally store the result in register number 0. (2pt)

Hint: here's a sample for loading value 3 into register number 0, and 2 into register 1 (one line per):

$OP_{2:0}$ = 011, $rd_{1:0}$ = 00, $in_{3:0}$ = 0011

$OP_{2:0}$ = 011, $rd_{1:0}$ = 01, $in_{3:0}$ = 0010

2. Register design:

A. Draw the circuit diagram of a D Flip-Flop with EN, using the `D flip-flop wo/SQ` component in the system library. Save it as a component in your library, as well as in a circuit file (`c1-1.cct`).
Requirement: your CCT file must show your component being tested using switches and probs.

B. Draw the circuit diagram of a 4bit Register using the above D Flip-Flop with EN, your register must have $D_3 D_2 D_1 D_0$, EN, C, and R as input ports, and $Q_3 Q_2 Q_1 Q_0$ as output (`c1-2.cct`).
Requirement: your CCT file must show your component being tested using switches, probs, and HEX Keyboard and Display.

3. Multiplexer design:

A) Design a 4bit 4-to-1 multiplexer, and show the component tested. (`c2.cct`).
Requirement: your CCT file must show your component being tested using switches and HEX keyboards/Displays.

4. Register array: draw the circuit diagram of a Register array with 4 registers, that meets the following specification (`c3.cct`):

A. The register array will have one 4bit `rd_in` bus providing new values to be stored, 2bit `rd` bus specifying the register to take in new values;

B. one 4bit `rs_out` bus outputting values from the register array, selected by the 2bit `rs` bus;

C. a single `Clear` switch that can clear all registers to 0; and

D. a single `CLK` switch simulating the clock unit.

E. you should use your own register in Q1, 2-to-4 decoder, 4channel 4bit multiplexer.
Requirement: your CCT file must show your component being tested using switches, probs, and HEX Keyboard and Display.