Jetic Gū

1. Handwritten submissions and proprietary formats (e.g. Pages or MS Word) **will not be graded**.
2. Late submission and resubmission policies are stated on the course webpage.
3. Mathematical expressions must be written entirely using LaTeX, otherwise **50%-100%** of marks will be deducted.
4. Circuits must be **tested** using switches/probs against a truth table. Untested circuits will receive 0.

Submission File structure:

```
submission.zip
    — answer.pdf
    — c1-1.cct
    — c1-2.cct
    — c3.cct
    — c6.cct
    — lib.clf
```

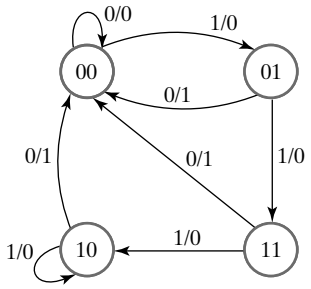
!**Important!**: for implementing the sequential circuit, you can use the `D flip-flop wo/SQ` component provided to you, just remember to connect all `R` pins to a single switch input called `Reset`.

# Lab 3

1. Save the library and circuit files we created in class containing the following designs in the final ZIP file (4pt):
   A. $SR$ latch with $C$ (`c1-1.cct`);
      Requirement: your CCT file must show the component being tested using switches and probs.
   B. $D$ flip-flop (`c1-2.cct`);
      Requirement: your CCT file must show the component being tested using switches and probs.
2. A sequential circuit has 2 D flip-flops $A$, $B$, and 2 inputs $X$ and $Y$. The circuit is described by the following input equations:
   $$D_A = \overline{X}A + XY, D_B = \overline{X}B + XA, Z = XB$$
   A. Derive the state table for the circuit (1pt).
   B. Derive the state diagram for the circuit (1pt).
3. You are tasked to design a 3bit counter, the counter will have three D Flip-Flops $A_2$, $A_1$, and $A_0$, for every single CLK pulse, its value increases by 1. Say at time 0, $A_2A_1A_0 = 000$, then the next time step it should be $001$, and the next $010$, so on.
   A. Assuming the next states are $D_2$, $D_1$, and $D_0$, derive the state diagram for the circuit (1pt).
   B. Assume you have an additional input $X$, which when it's equal to 1 changes the next state to 000 regardless of current state. Find the boolean expressions (1pt), then draw the circuit diagram and save it as `c3.cct` (3pt).

Requirement: you must show the implemented component tested using a switch for $X$, and a Hex display for showing the current state.

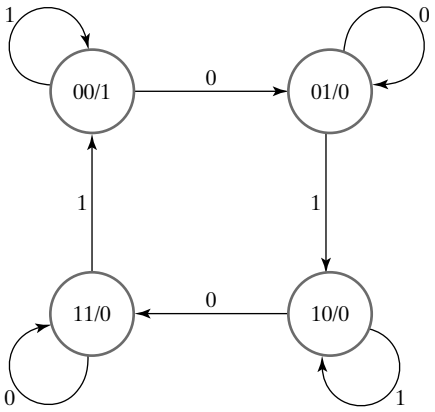
4. For the following state diagram.




   A. Starting from state 00 in the following state diagram, show the state transition sequence and output sequence for input sequence 0101101111 (1pt).

   B. Draw the state table, perform flip-flop input equation determination and output equation determination (1pt).

5. A sequential circuit has two flip-flops $A$ and $B$, one input $X$, and one output $Y$. The state diagram is shown in the following figure. Draw the state table (1pt).




6. Draw the state diagram of the following rotator, write down the equations for each $D$ flip-flop (1pt), and complete the implementation as `c6.cct` (3pt). You should make it so that $X_3X_2X_1X_0$ are 4bits of input controlled using a HEX Keyboard.

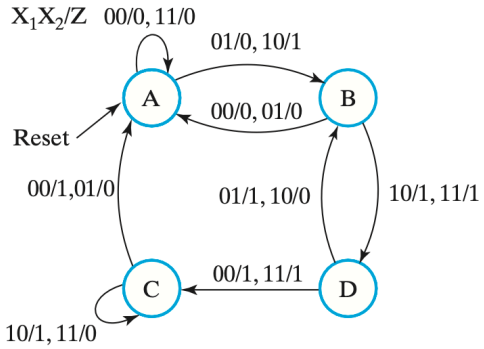
   **Input** $Y$

   0: The next state should equal to current input $X_3X_2X_1X_0$;

   1: The next state should equal to the current state, right rotated rightwards once (e.g. for current state $X_3X_2X_1X_0$, the next state should be $X_0X_3X_2X_1$);

7. Work on the following state diagram.

   (1) Draw the state-machine diagram (1pt).




(2) Perform state assignment, write down the Flip-Flop Input Equations and Output Equations, then optimise it (1pt).

(3) ~~Implement the circuit, save as `c7.cct` (2pt).~~ This is removed from requirement for Lab 3, as of 2024 Fall.