05.04.21 12:00

CSCI 150
Introduction to Digital and Computer System Design
Lecture 5: Registers IV

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Overview

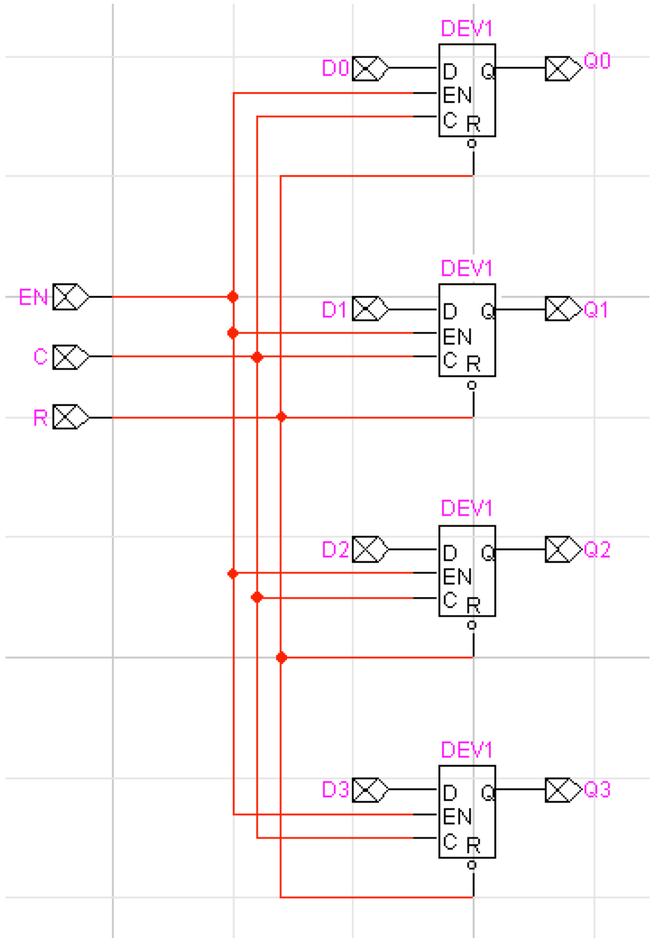
- Focus: Fundamentals of Complex Digital Circuit Design
- Architecture: von Neumann
- Textbook v4: Ch7 7.6; v5: Ch6 6.6
- Core Ideas:

  1. Lab, Lab, Lab, Lab

P1
4-bit Register

Implementation of 4-bit Register

- Use D flip-flop EN wo/ SQ/ from system library for simplicity
  - You can use your own implementation using gates, but it will be more complicated and slower in simulation
- Inputs: D3, D2, D1, D0, EN, C, R;
  Output: Q3, Q2, Q1, Q0

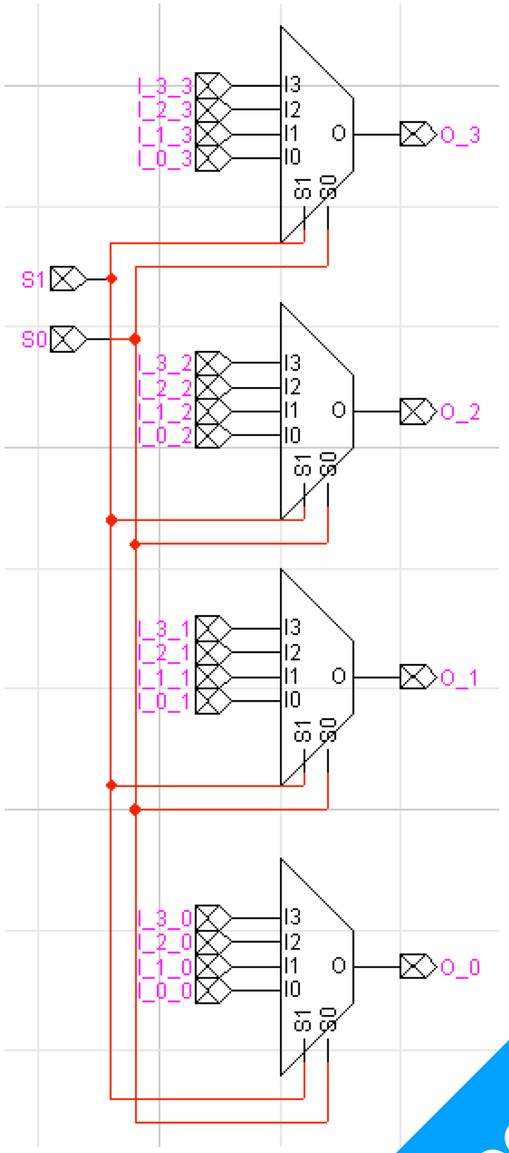


Technical

P1
4-bit Register

Implementation of 4-bit 4-to-1 Multiplexer

- First, implement 1-bit 4-to-1 Multiplexer
- Use 4 x 1-bit 4-to-1 Multiplexers to implement the 4-bit 4-to-1 Multiplexer
- Make sure your wires and I/O names are correct!



Technical

P1
4-bit Register

Implementation of Register Array

- 4 x 4-bit registers
- Single Output Lane: O3, O2, O1, O0 through Multiplexer
  (use `Hex Display`)
- Single Input Lane: I3, I2, I1, I0
  For new values (use `Hex Keyboard wo/ STB`)
- Address for output lane: Add_Out_1, Add_Out_0
  (use `Hex Keyboard wo/ STB`)
- Address for input lane: Add_In_1, Add_In_0
  (use `Hex Keyboard wo/ STB`)
- Connect unused pins to digital ground (`DGND`)
  to prevent errors

Technical

P1
4-bit Register

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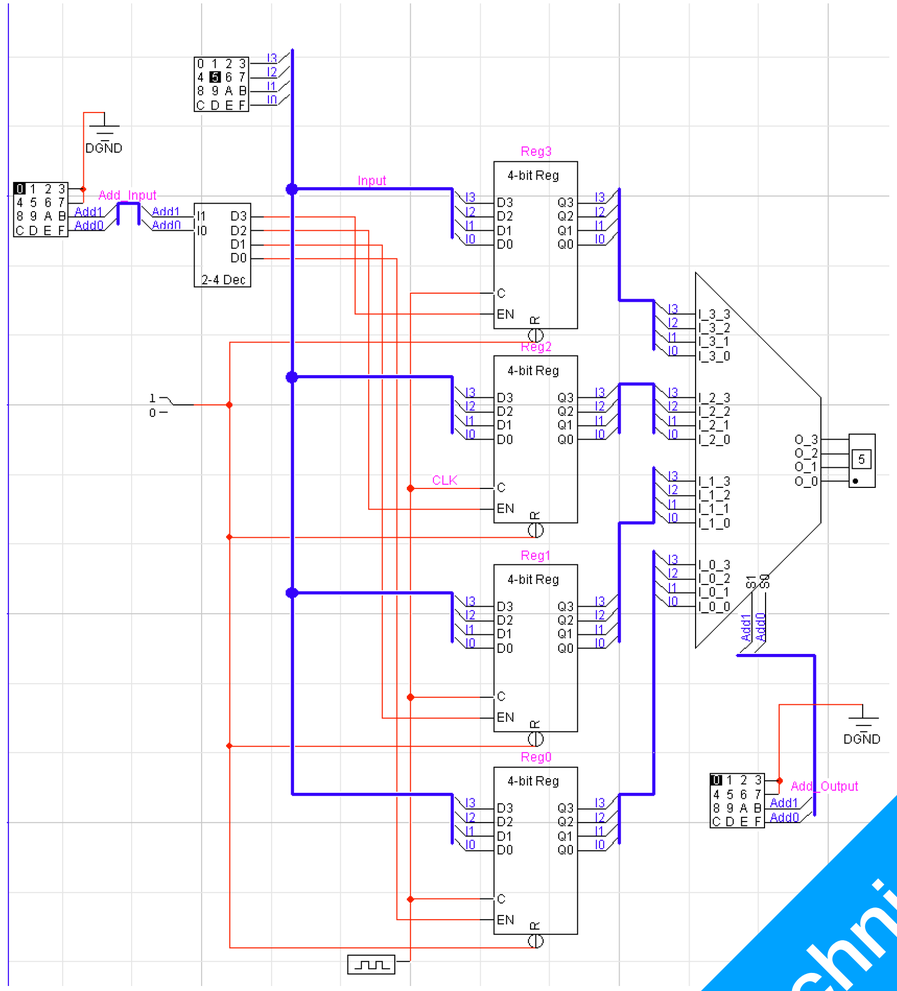

Technical