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CSCI 150
Introduction to Digital and Computer System Design
Lecture 4: Sequential Circuit VI

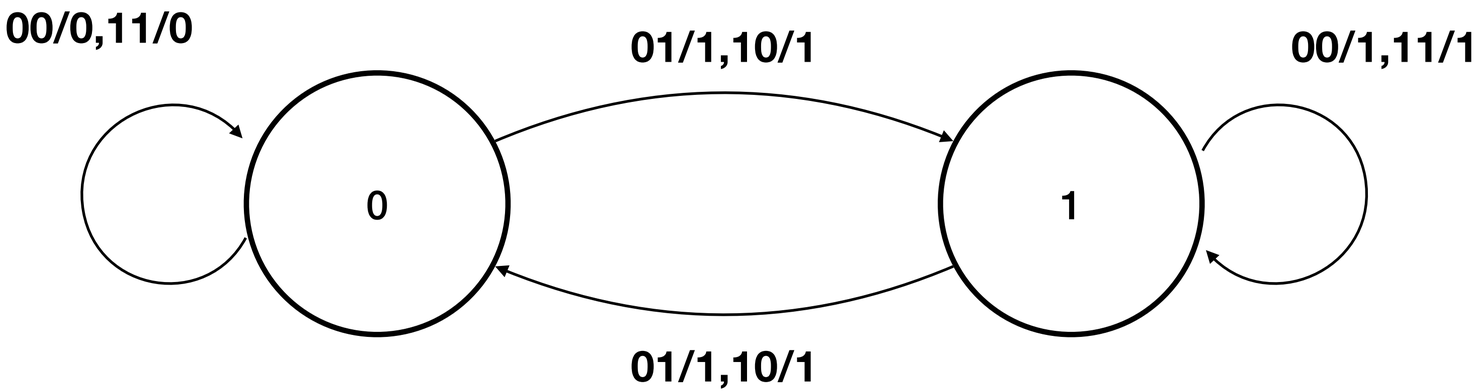
Jetic Gū

Overview

- Focus: Basic Information Retaining Blocks
- Architecture: Sequential Circuit
- Textbook v4: Ch5 5.7; v5: Ch4 4.6
- Core Ideas:
    1. State Machine Diagrams: Moore model

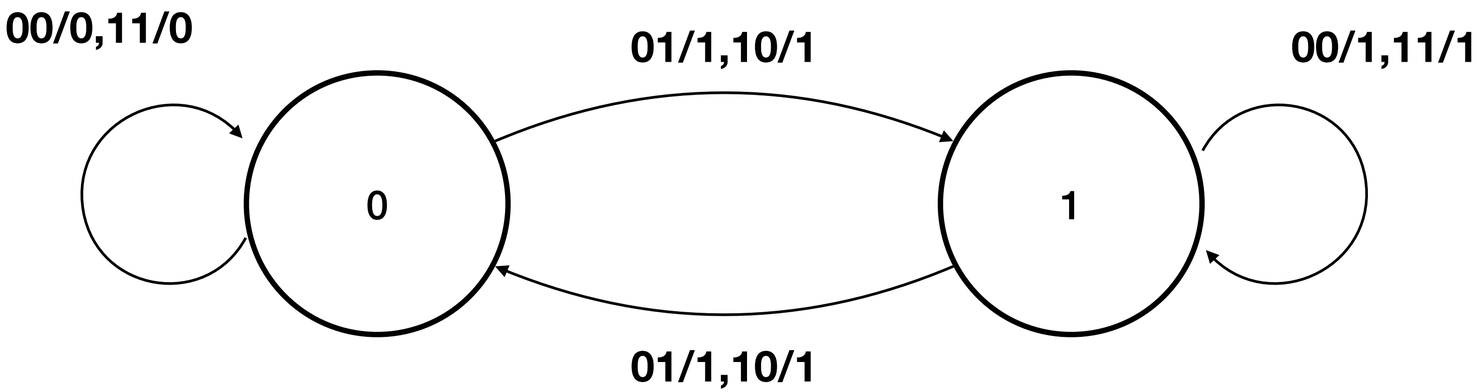
P0
Review

State Diagram



Review

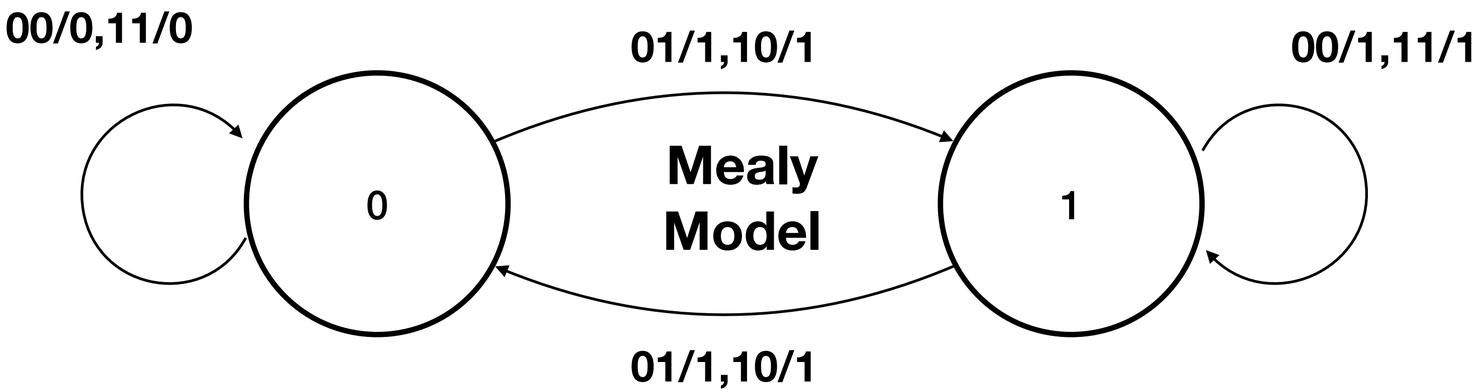
State Diagram



Mealy machine: a **finite-state machine** whose output values are determined both by its current state and the current inputs

P0
Review

State Diagram



Mealy machine: a **finite-state machine** whose output values are determined both by its current state and the current inputs

Review

P0
Review

State Diagram

- Modelling state transitions in a visual way
- Problems with Mealy Model
  - Inefficient when input and output contain too many bits
    all 2^n inputs and m-bit outputs must be written down for each transition
  - Unworkable for larger designs

Review

State Machine Diagrams

Moore Model

Summary

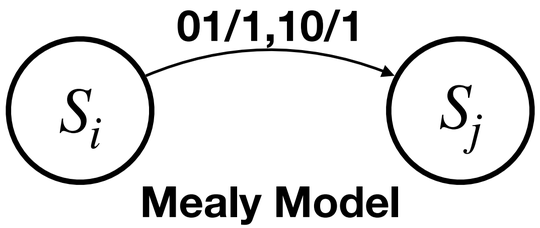
Improvements over Mealy

- Called Moore, the name sounds better
  (also State-Machine Diagram)

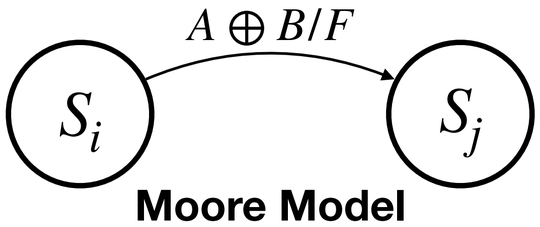
- Conditions

  - Input Condition: Boolean expressions or equations
    Also called **transition condition (TC)**, causes transition when its value is 1

  - **Output Condition (OC)**: Boolean expressions or equations
    Causes specific output when its value is 1



Mealy Model

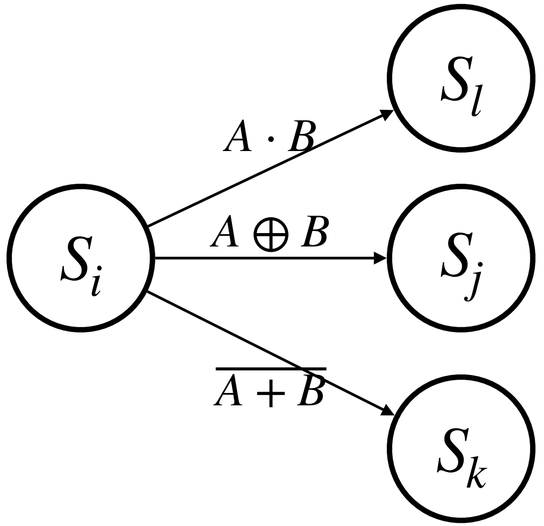


Moore Model

Concept

Transition Conditions

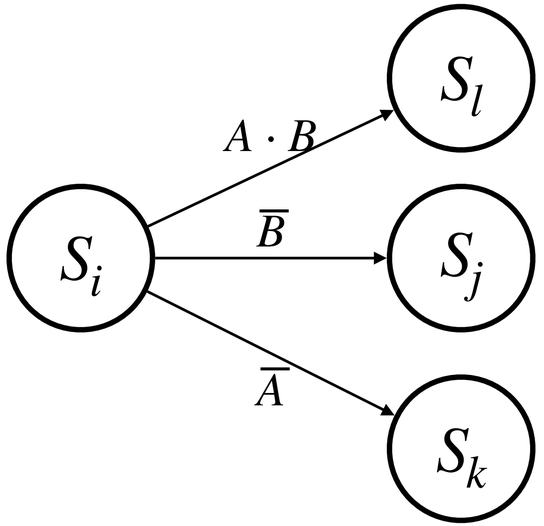
- Associated with transitions
- Performs transition when condition is met
- Validity
  Must not be conflicting conditions
  i.e. only one TC can be true for any given input



Concept

Transition Conditions

- Invalid TC
  - Condition $\overline{A}$ and $\overline{B}$ can be met at the same time
- Check all transitions from each state of invalid TC

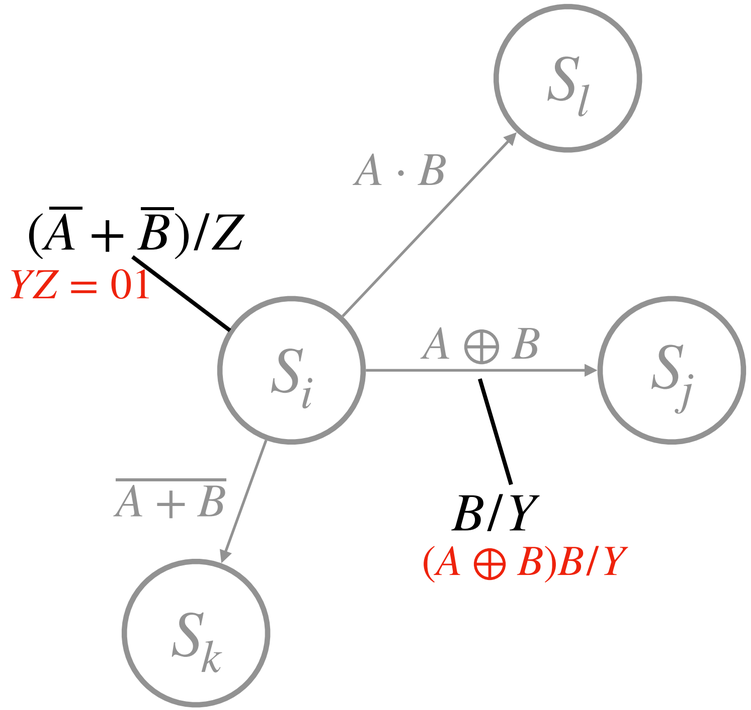


Concept

Output Conditions

Defaults: $Y = 0, Z = 0$

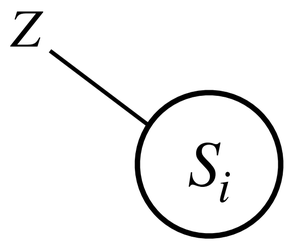
- Associated with transitions/states
- For associated transition/state, outputs when condition is met
- Default: output values unless otherwise specified
- Validity
  Must not be conflicting conditions
  i.e. only one OC can be true for any given input/state



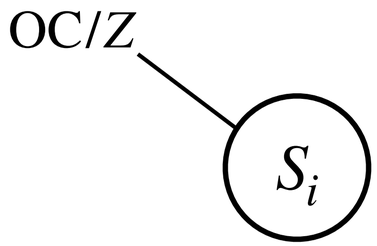
Concept

Output Conditions

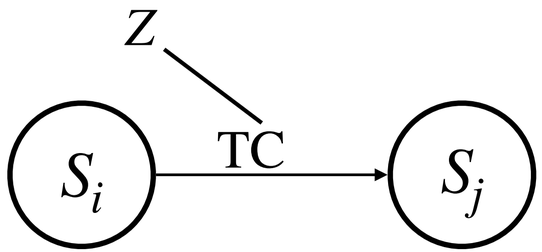
Defaults: $Y = 0, Z = 0$



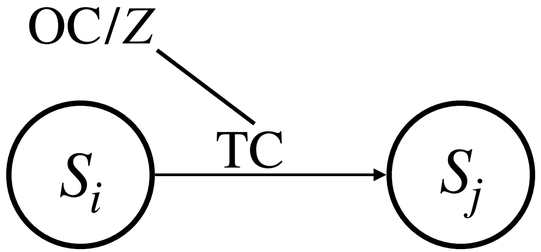
Always output 01 at state S_i



Output 01 when condition OC is met at S_i



Always output 01 at state S_i, when input meets TC



Output 01 when condition OC is met at S_i, and input meets TC

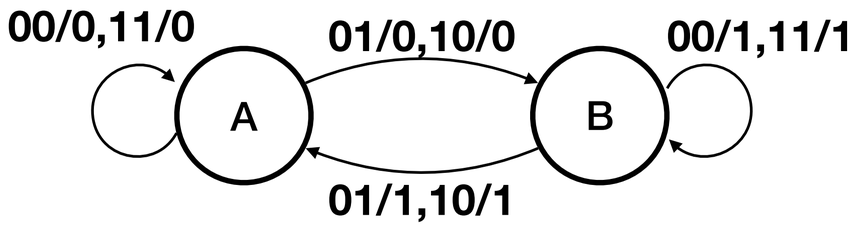
Concept

Output Conditions

- Invalid OC
  - Condition $\overline{A}$ and $\overline{B}$ can be met at the same time
- Check all transitions from each state of invalid OC

Concept

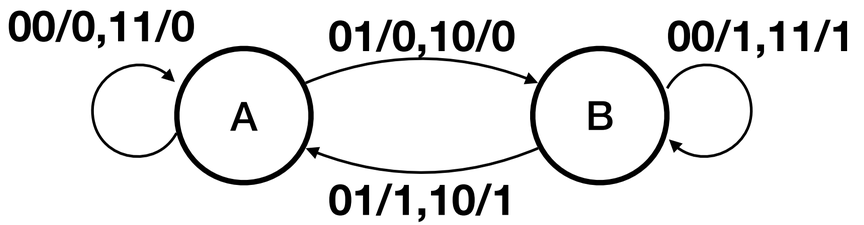
From Mealy to Moore



1. Preserve arcs
2. Do the TCs
3. Do the OCs

Example

From Mealy to Moore



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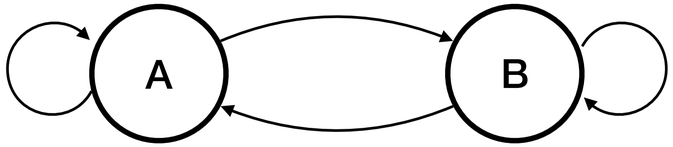

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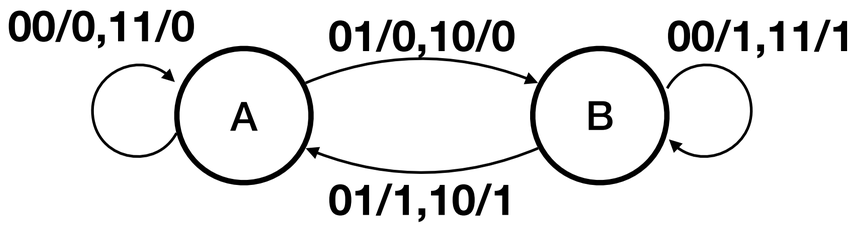

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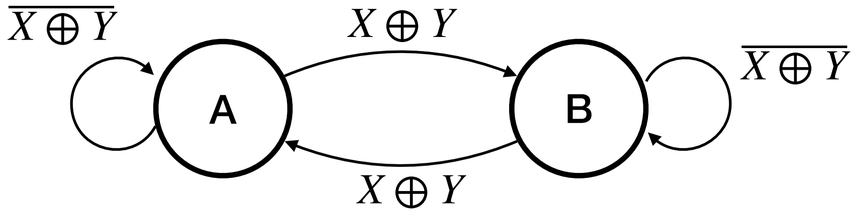

Example

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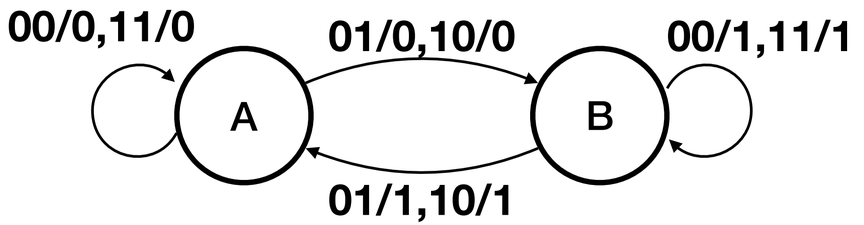
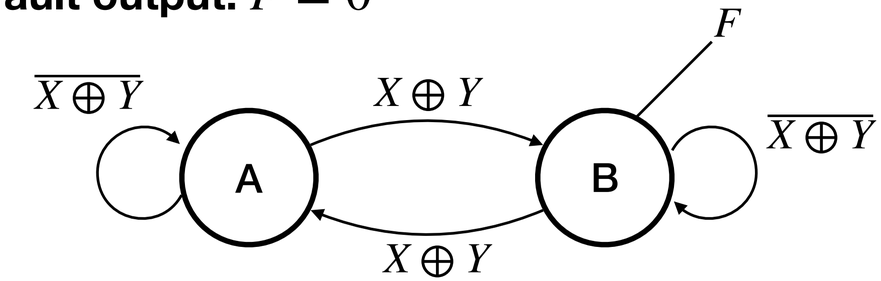


1. Preserve arcs
2. Do the TCs
3. Do the OCs

Default output: $F = 0$



Example

P1
State-Machine

From State Table to Moore

State Table

Present State		X	Next State		F
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

Exercise

P1
State-Machine

From State Table to Moore

State Table

Present State A	Present State B	X	Next State A	Next State B	F
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

Input: X
Output: F
Default: $F = 0$

Exercise

P1
State-Machine

From State Table to Moore

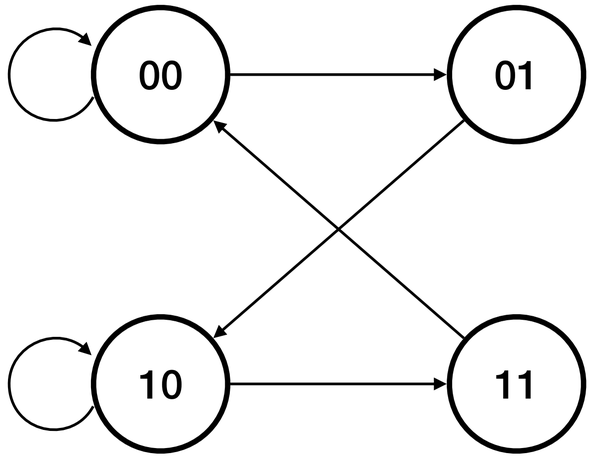
State Table

Present State A	Present State B	X	Next State A	Next State B	F
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

Input: X

Output: F

Default: $F = 0$



Exercise

P1
State-Machine

From State Table to Moore

State Table

Present State A	Present State B	X	Next State A	Next State B	F
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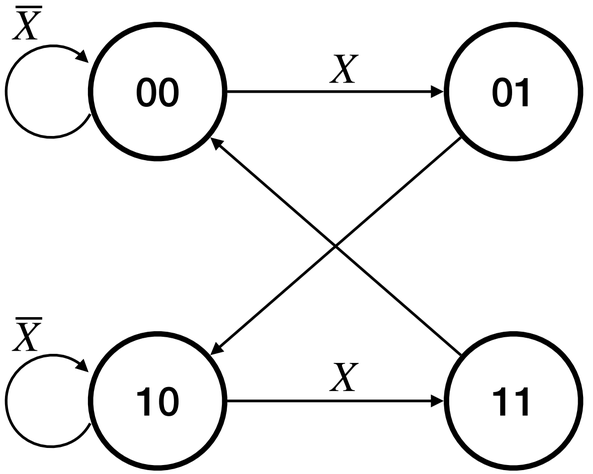
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	0	0	0

Input: X

Output: F

Default: $F = 0$



Exercise

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From State Table to Moore

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Input: X

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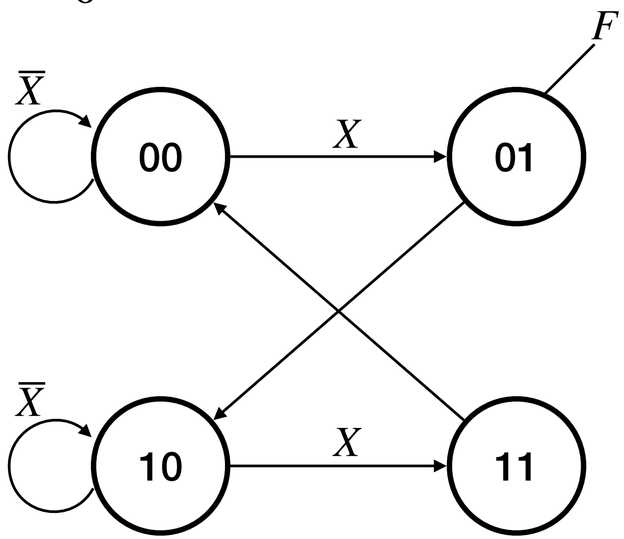
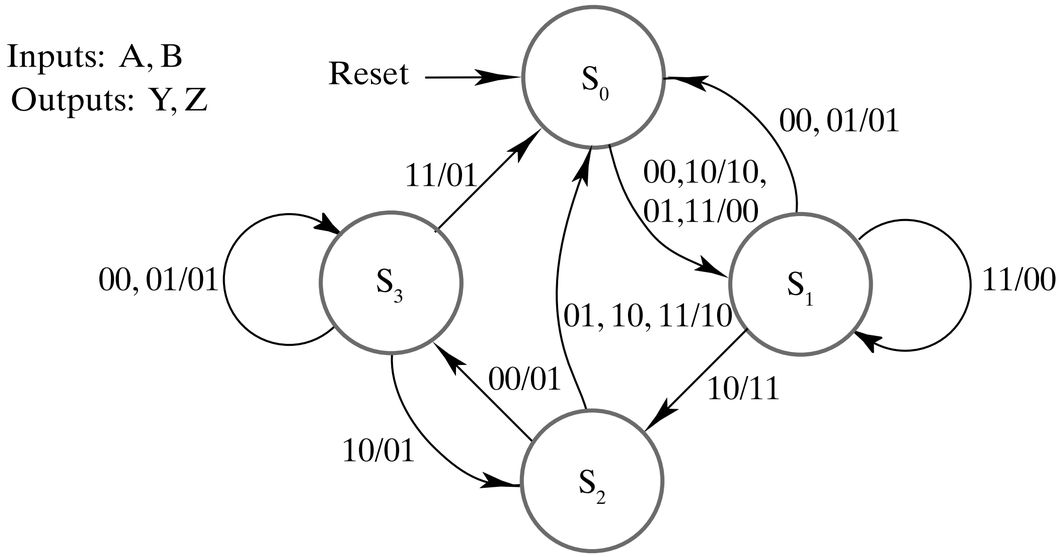


Exercise

P1
State-Machine

From Mealy to Moore



Exercise

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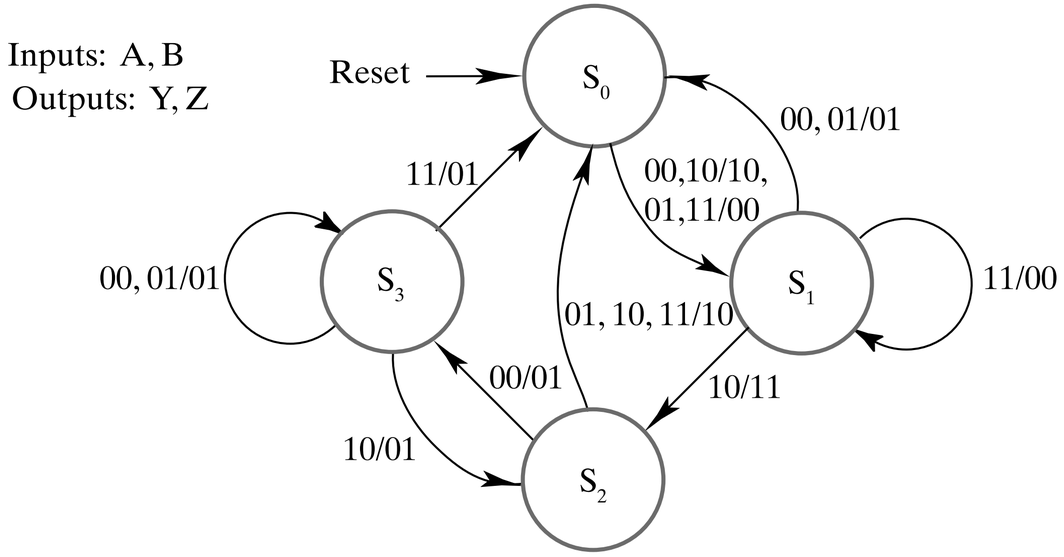

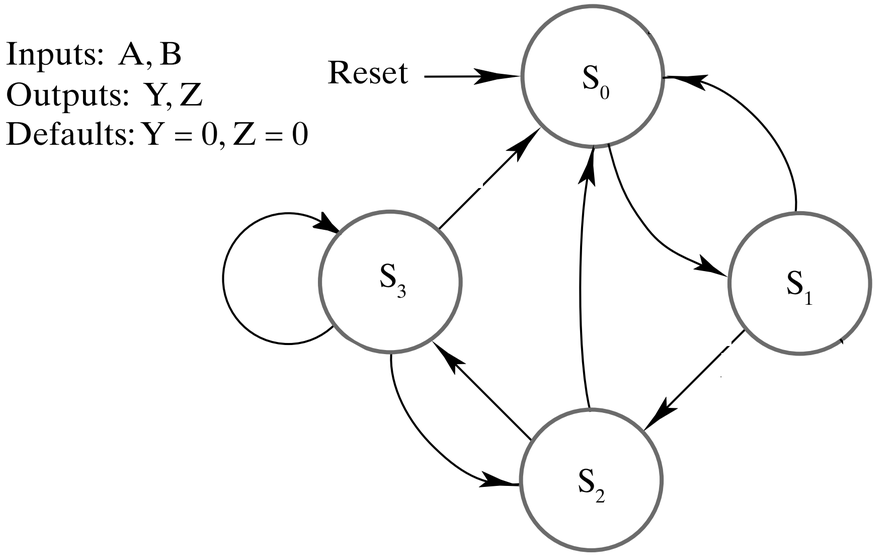

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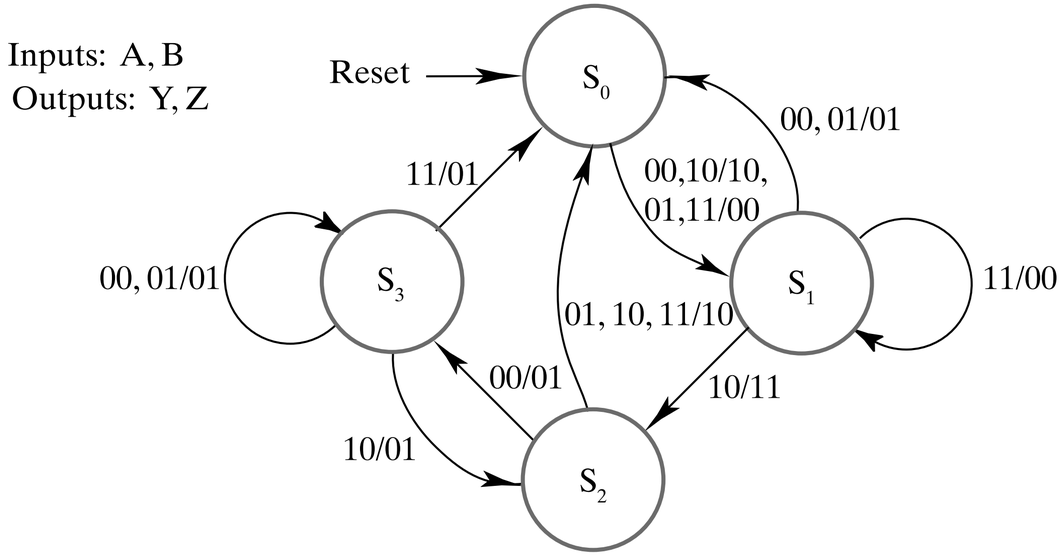
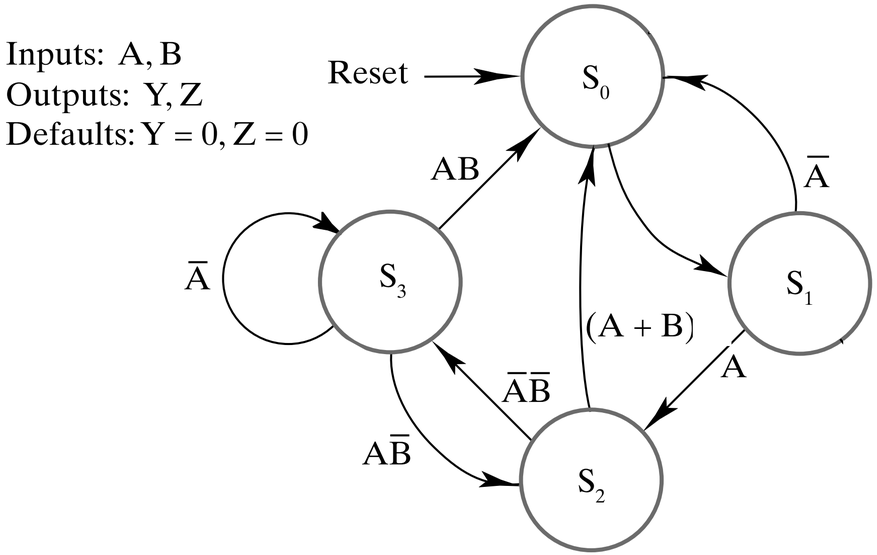
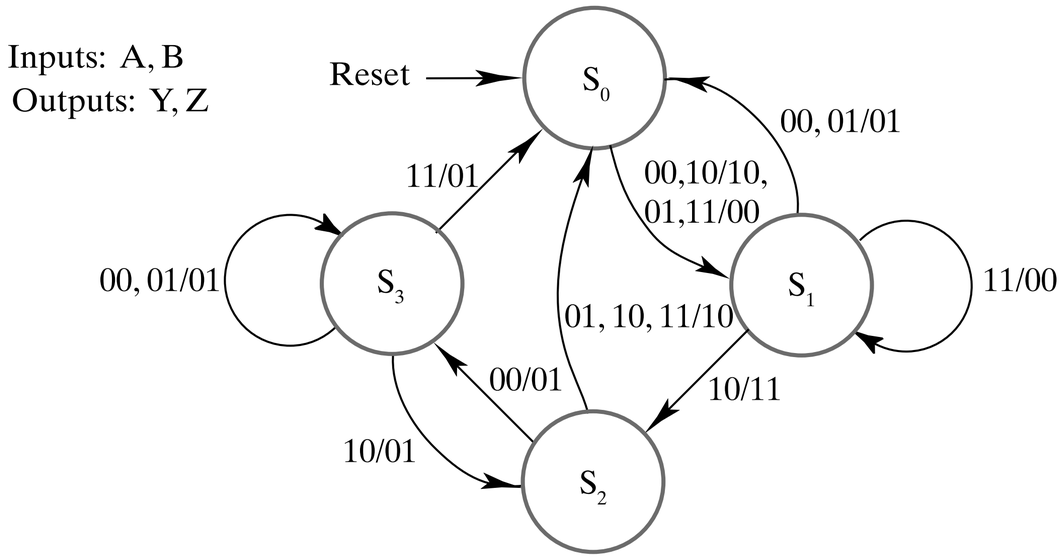


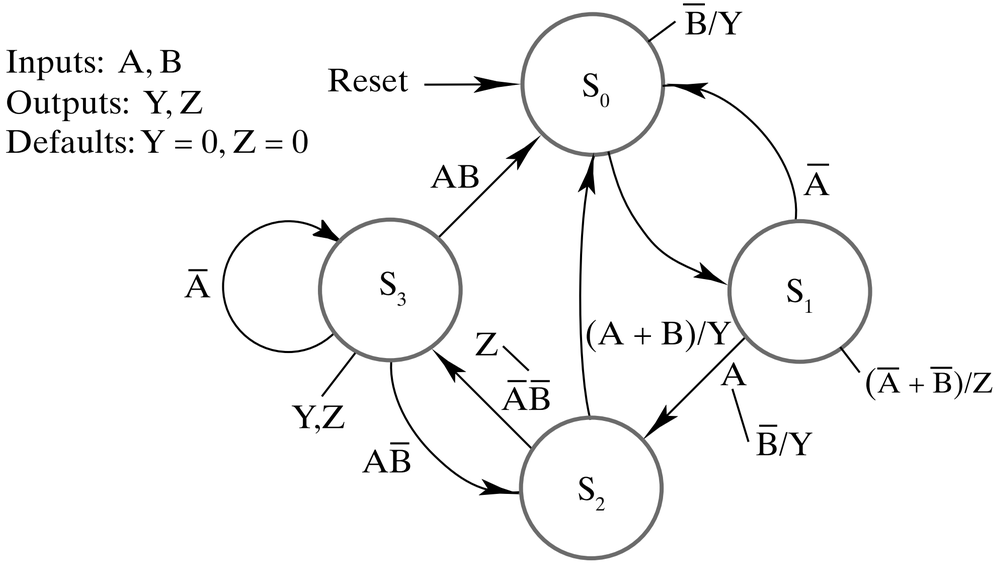


Exercise

P1
State-Machine

From Mealy to Moore





Exercise