CSCI 150
Introduction to Digital and Computer System Design
Lecture 2: Combinational Logical Circuits V

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Overview

- Focus: Boolean Algebra

- Architecture: Combinatory Logical Circuits

- Textbook v4: Ch2 2.8, 2.9. 2.10; v5: Ch2 2.6, 2.7

- Core Ideas:

  1. Other Gate Types: XOR, NAND, NOR, Buffer, High-Impedance, Odd Function

  2. Lecture 2 Review

Boolean Algebra I-III

I. AND, OR, NOT Operators and Gates

- Simple digital circuit implementation

- Algebraic manipulation using Binary Identities

II. Standard Forms

- Minterm & Maxterm

- Sum of Products & Product of Sums

III. Optimisation Using K-Map (For 2,3,4 Variables)

Review

Other Gate Types

Delay Propagation
XOR, NAND, NOR, Buffer

Gate Delay

Timing Diagram (REALITY)

X ——

Y ——

$Z = X \cdot Y$

X

1

| 0 | 1 | 0 | 1 | 0 |

Y

1

| 0 | 0 | 1 | 1 | 0 |

Z

1

| 1 |

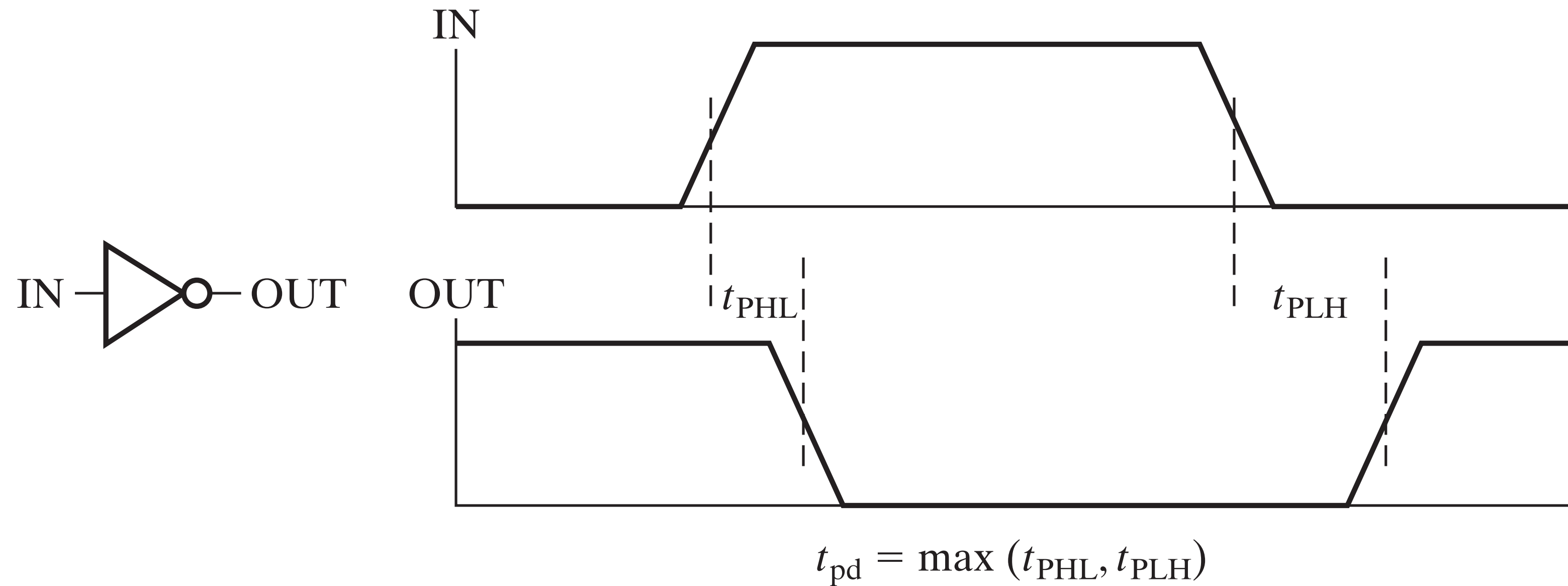**Gate delay** t_G

0   1   2   3   4   5
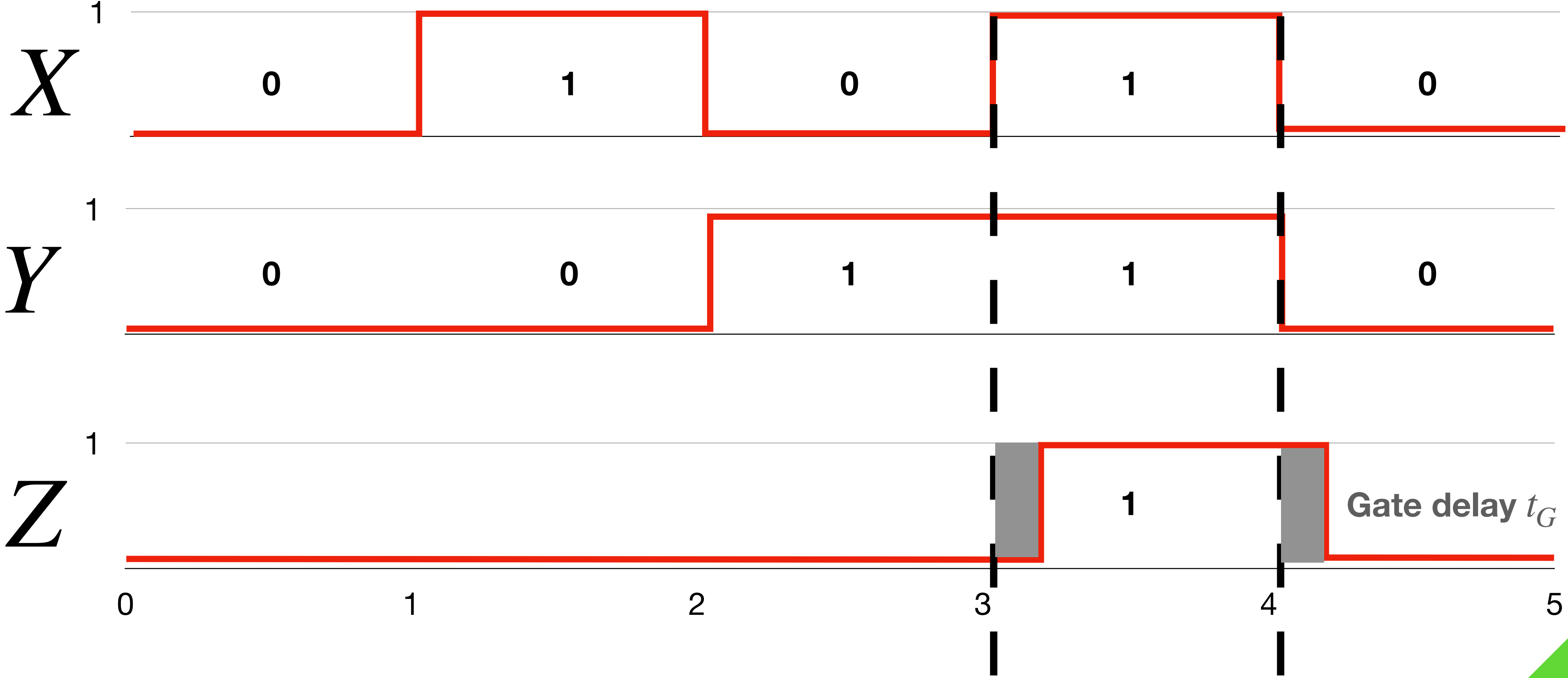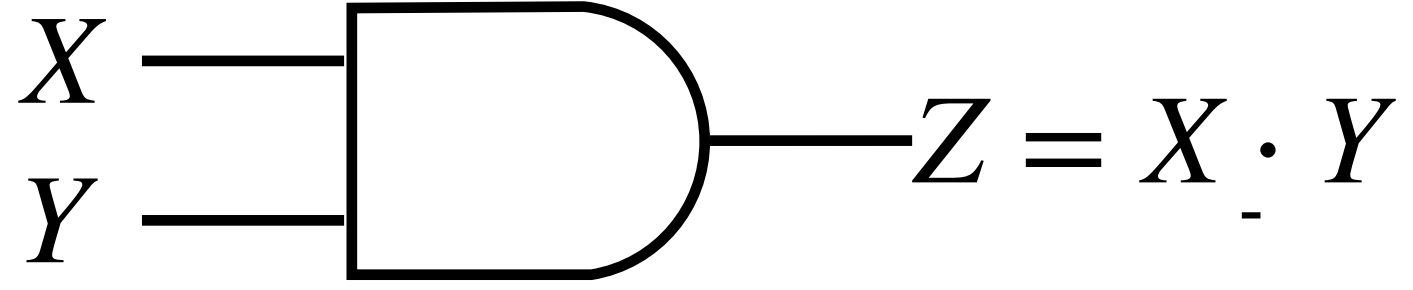
Review

Delays

- Gate Delay

  - The time required for a change in value of a signal to propagate from input to output (of a Gate)

- Propagation Delay

  - The time required for a change in value of a signal to propagate from input to output (of a Circuit)

Delays

$$t_{\mathrm{pd}} = \max\left(t_{\mathrm{PHL}}, t_{\mathrm{PLH}}\right)$$

- t_{pd}: Propagation Delay: longest time for propagating from input to output

- t_{PHL}: Hight2Low propagation time; t_{PLH}: Low2High propagation time;
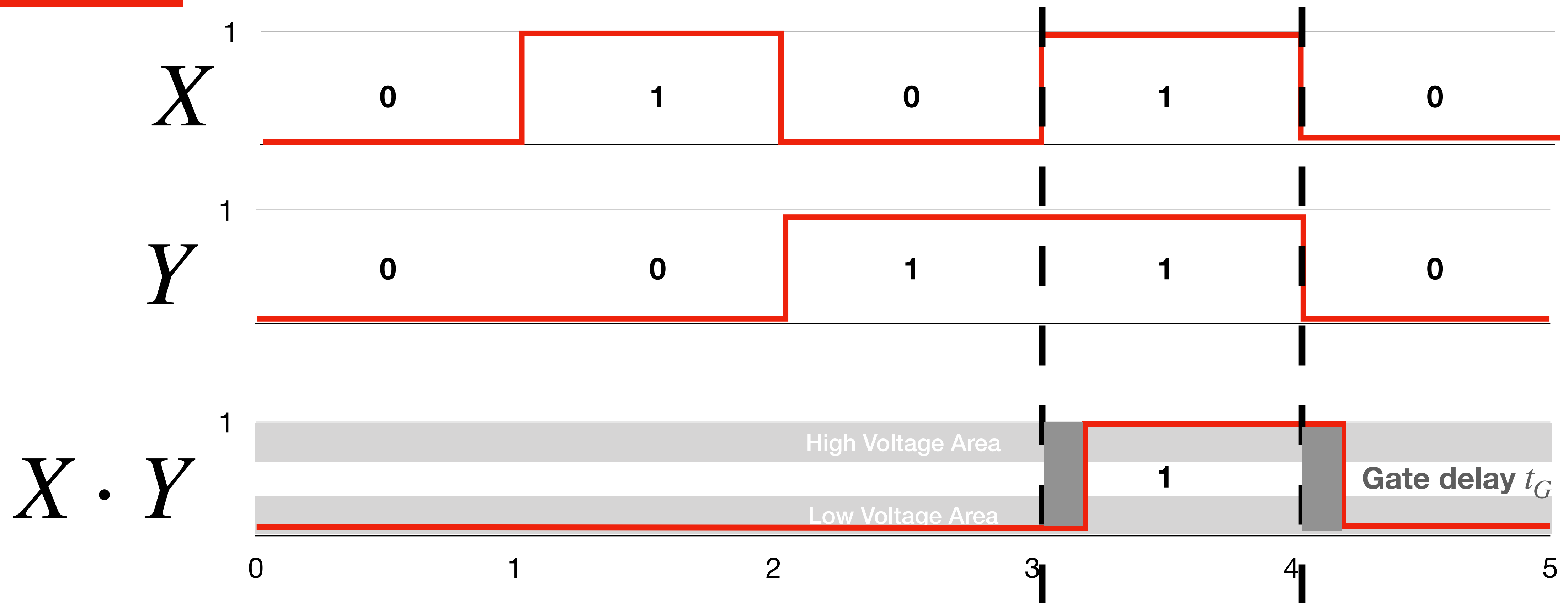
Concept

Transport and Inertial Delays
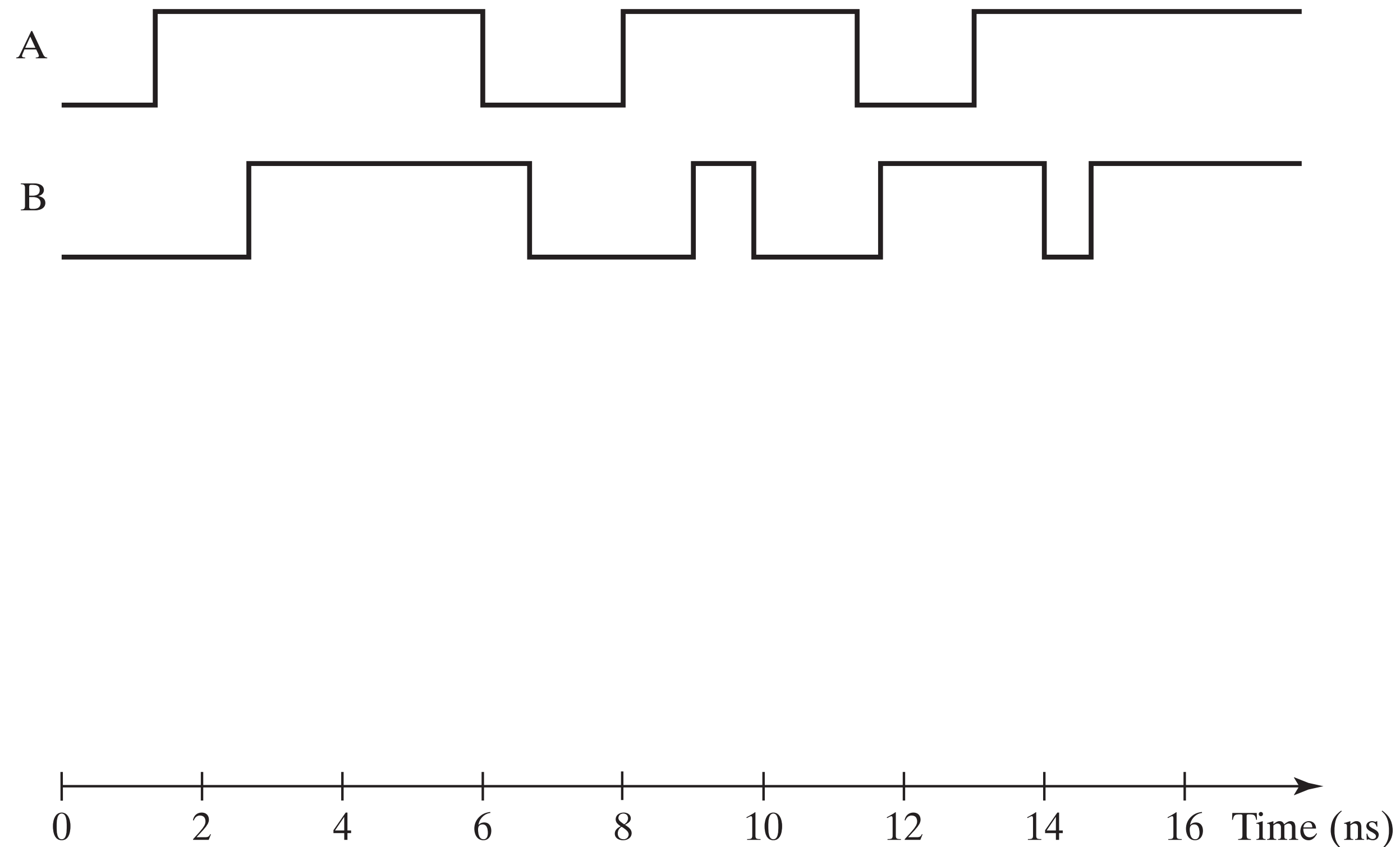
- **Transport Delay**: output in response to input changes after propagation delay

- **Inertial Delay**: if a value changes twice in a short time (**rejection time**), ignore

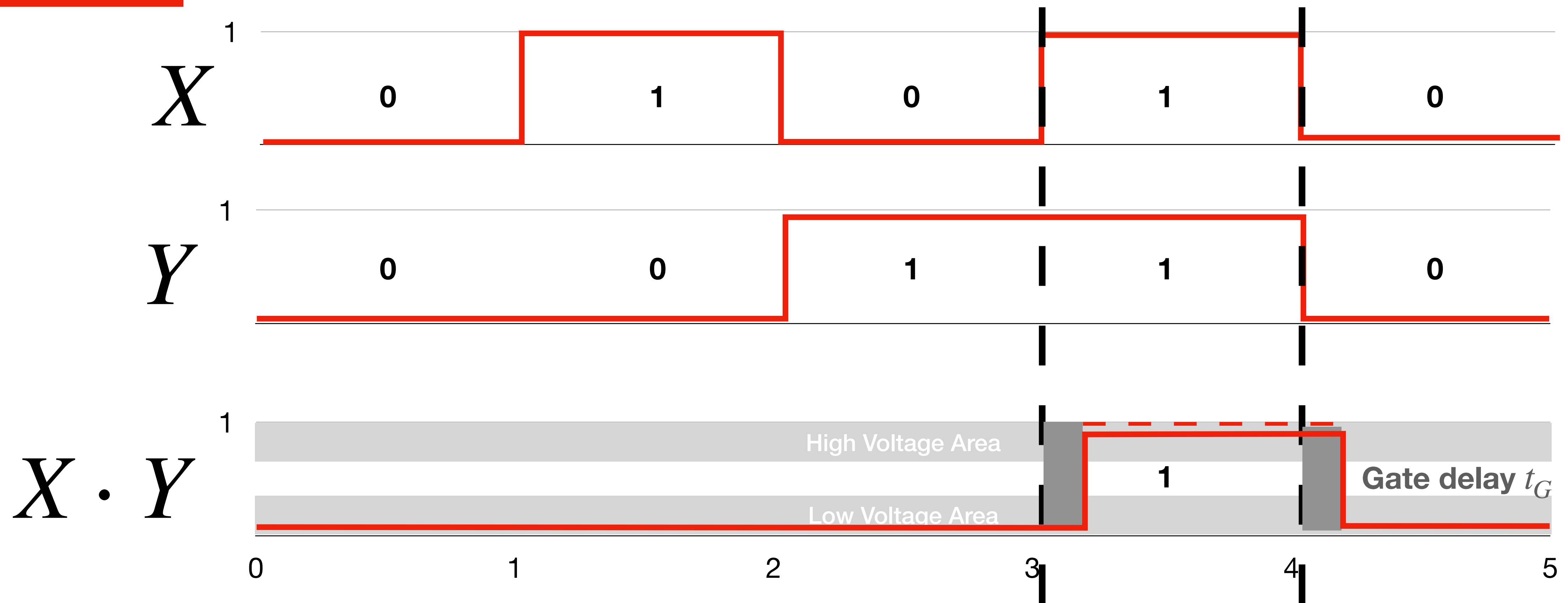# Parameters of Gate Delay

- Fan-in
  number of inputs of a logic gate

- Fan-out (standard load)
  number of gates that each logic gate can drive while providing voltage levels
  in the guaranteed range is called the standard load or fan-out

Concept

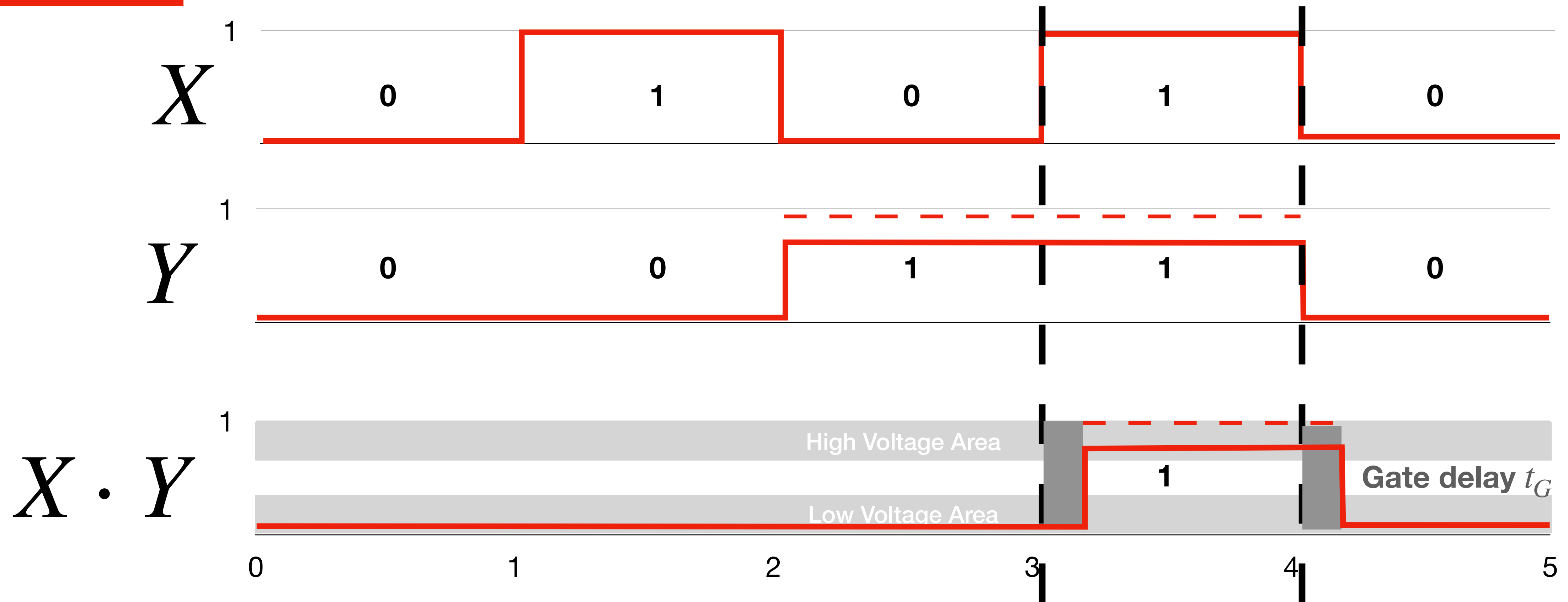# Standard Load

X

| 0 | 1 | 0 | 1 | 0 |

Y

| 0 | 0 | 1 | 1 | 0 |

$X \cdot Y$

High Voltage Area

| 1 |

Low Voltage Area

Gate delay t_G

0   1   2   3   4   5

- Digital circuits are driven by power, each component also takes power

Demo

Standard Load

X

1

0   1   0   1   0

Y

1

0   0   1   1   0

$X \cdot Y$

1

High Voltage Area

1

Low Voltage Area

Gate delay t_G

0   1   2   3   4   5

- Digital circuits are driven by power, each component also takes power

Demo

Standard Load

- Changes in input voltage can also affect output voltage

Standard Load

X

| 0 | 1 | 0 | 1 | 0 |

Y

| 0 | 0 | 1 | 1 | 0 |

$X \cdot Y$

High Voltage Area

1

Low Voltage Area

Gate delay t_G

0   1   2   3   4   5
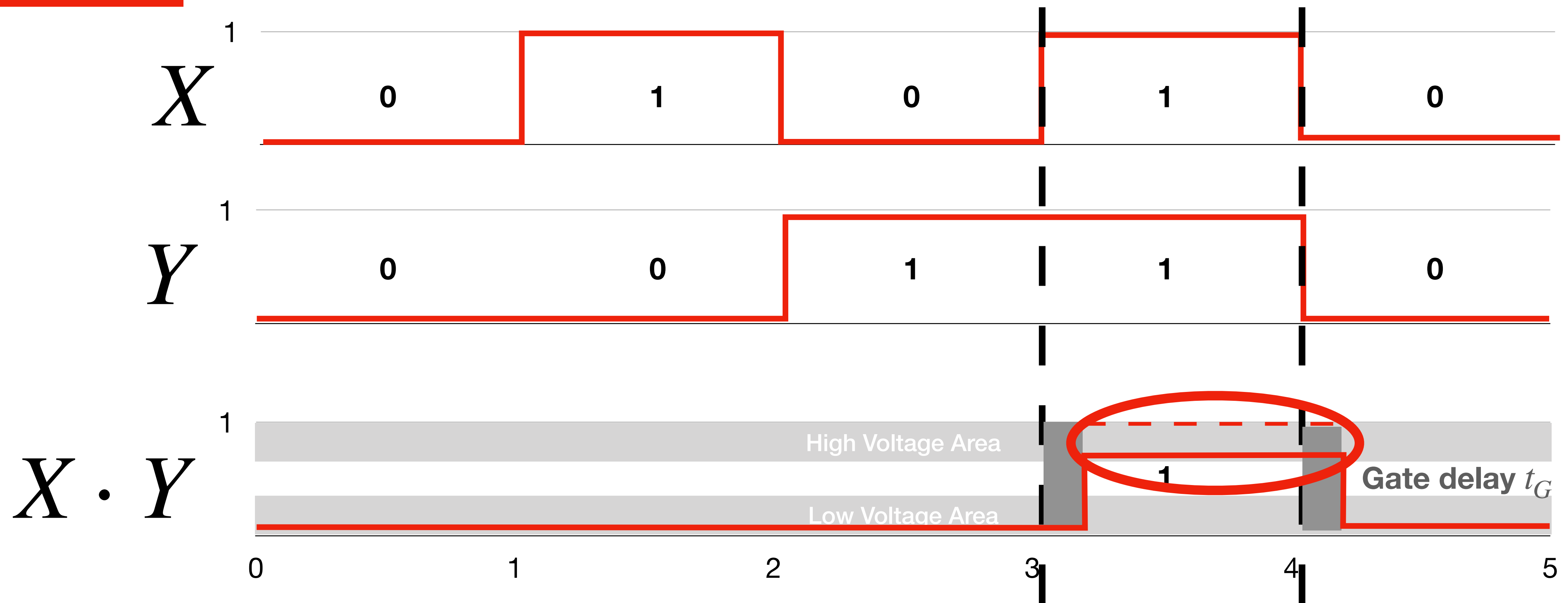
- If it takes too much power, it will not be able to guarantee output voltage

- Standard load is defining that power consumption, which also affect delay

Demo

Standard Load
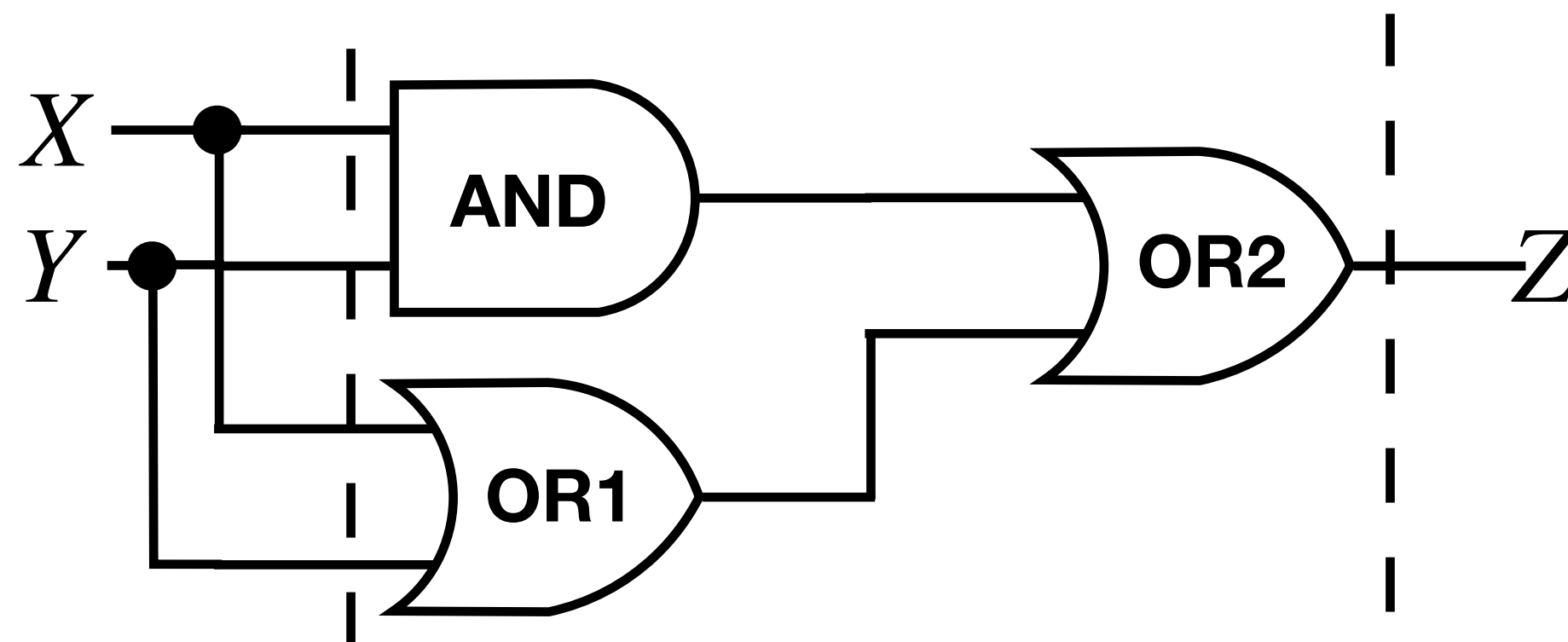
- OR Gate: 0.8 SL; AND Gate: 1.00 SL;

- Delay for AND:
$$t_{pd} = 0.07 + 0.021 \times \sum InputSL$$

- Delay for OR:
$$t_{pd} = 0.05 + 0.02 \times \sum InputSL$$

- Estimation for OR2
$$t_{pd} = 0.05 + 0.02 \times (0.8 + 1.00) = 0.086\text{ns}$$

- Precise estimation is very hard, since we lack a lot of these information

- We can ignore this computation, but you should know roughly

Demo

Other Gates

XOR Gate Exclusive-OR

$$Z = X \oplus Y$$

Buffer

$$Z = X$$
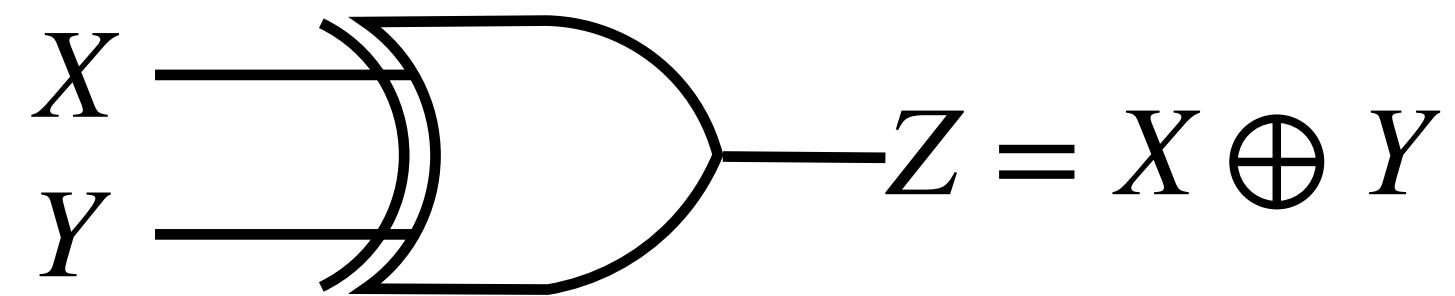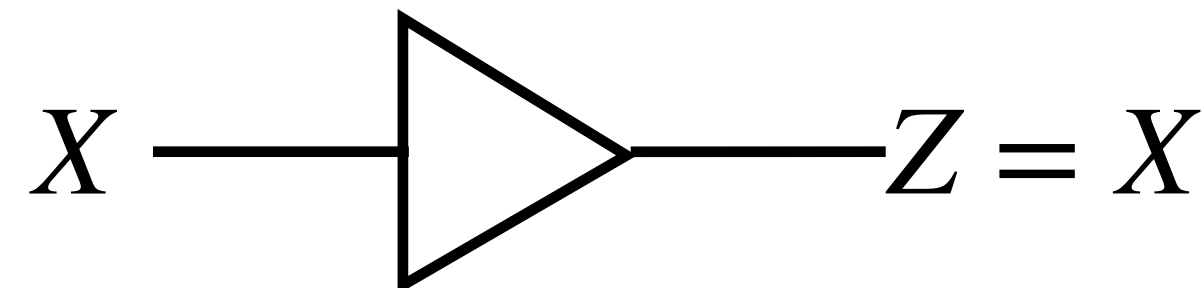
3-State Buffer

Buffer

**XOR Gate
Exclusive-OR**
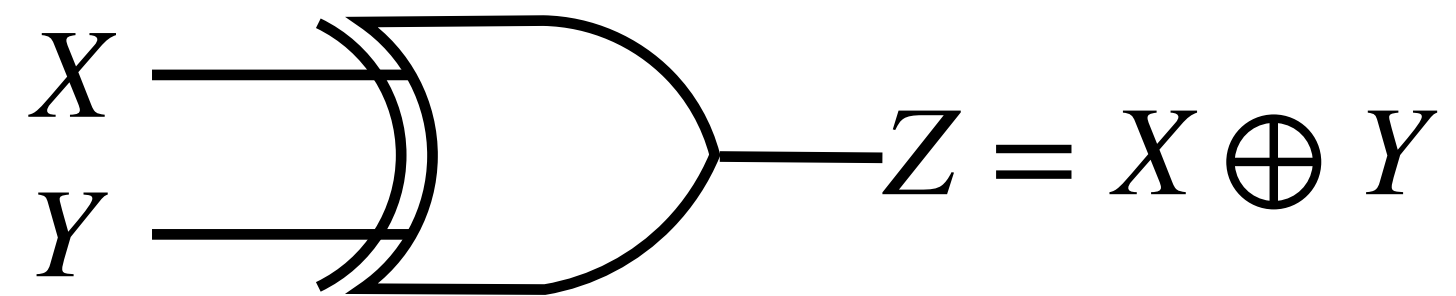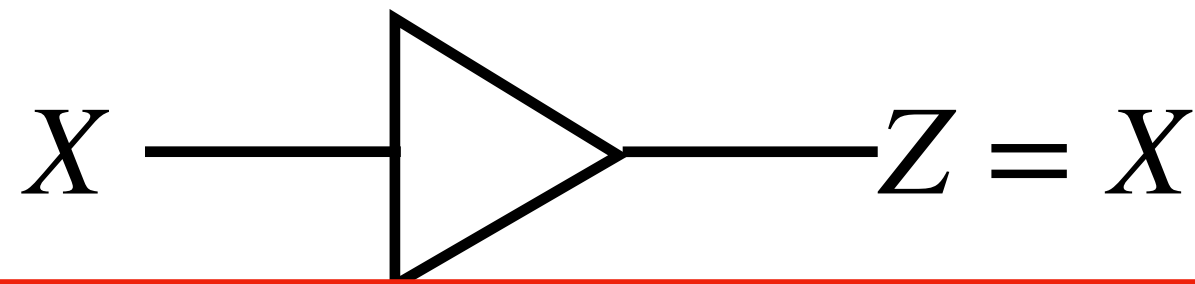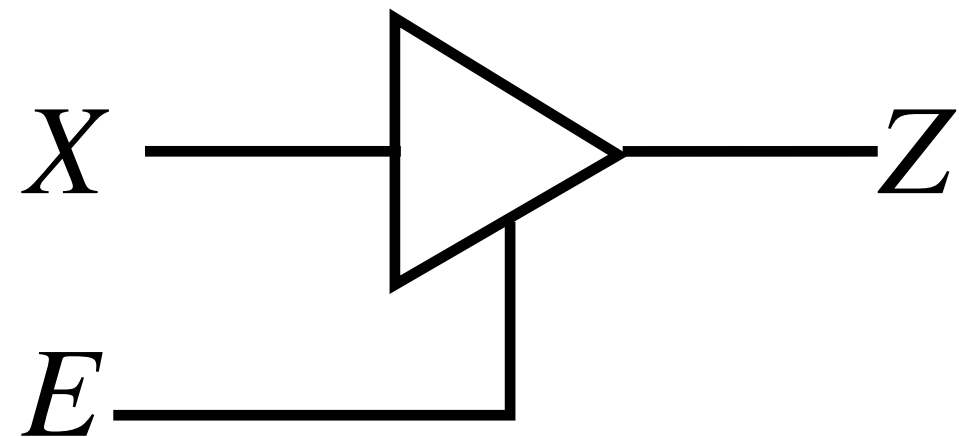
X
Y
$Z = X \oplus Y$

Buffer

X — $Z = X$

3-State Buffer

X

E

Z

- Has delay

- Increases output Voltage
  e.g.: input 0.8 V, output 1.0 V

Concept

3-State Buffer

**XOR Gate
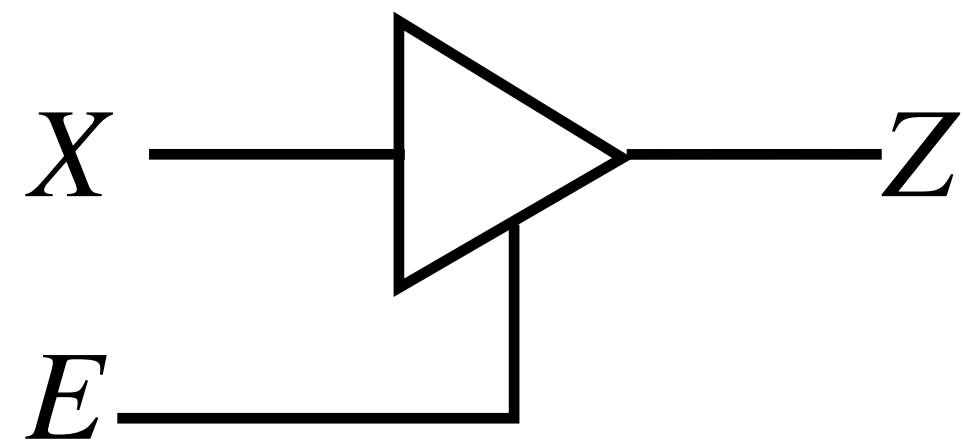Exclusive-OR**

X
Y
$Z = X \oplus Y$

Buffer
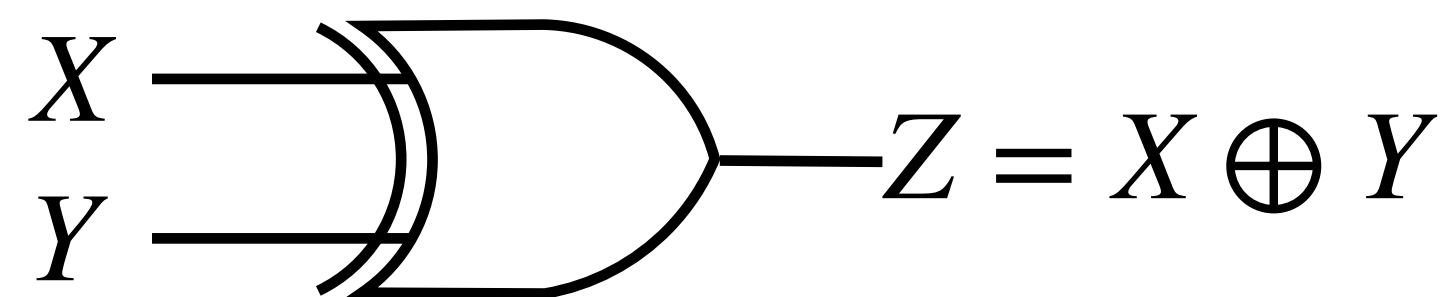
X —▷— $Z = X$

3-State Buffer

X
E
Z
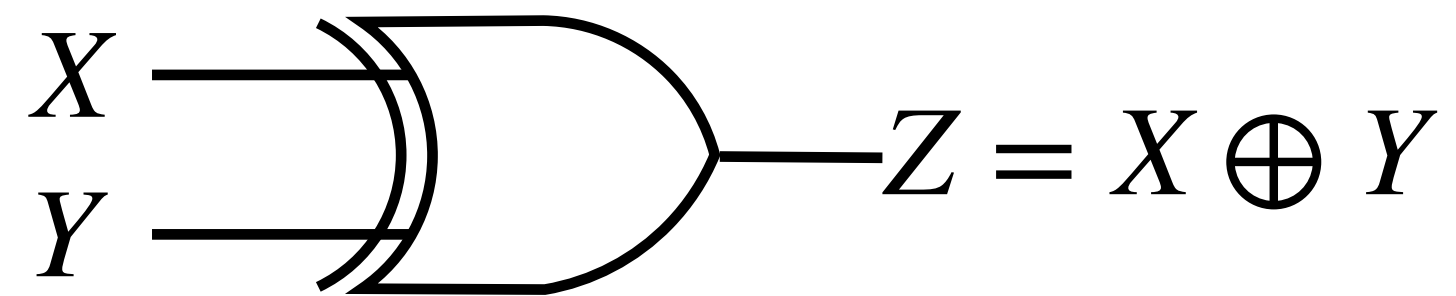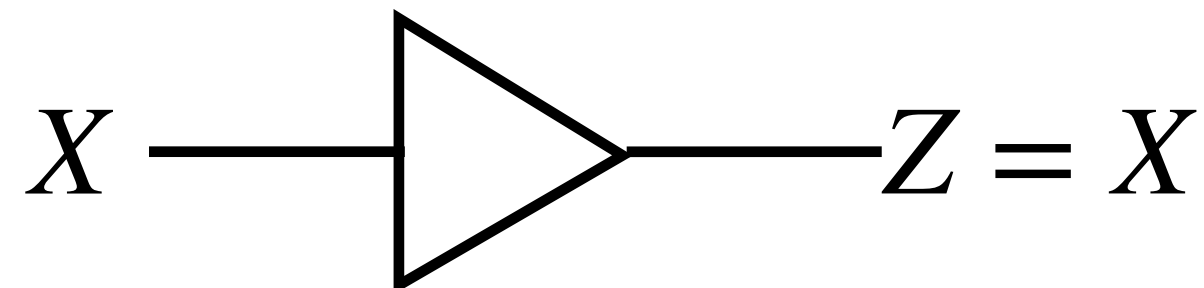
- Has delay

- Increases output Voltage
  e.g.: input 0.8 V, output 1.0 V

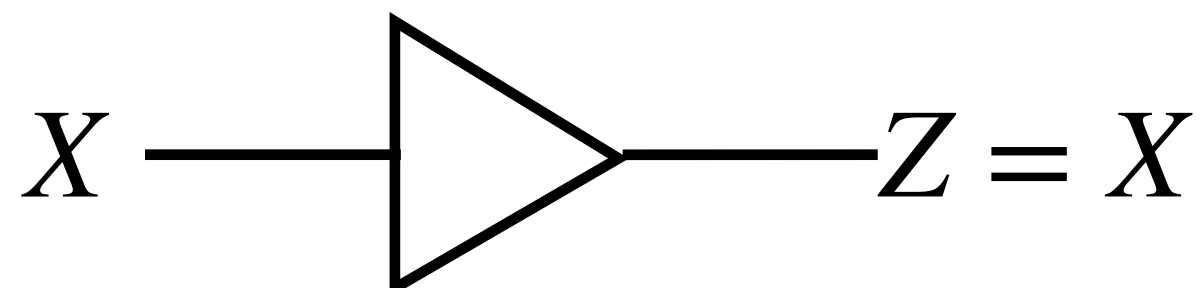- When $E = 0$, outputs no electricity
  (Open circuit/Hi-Z/High Impedance)

Concept
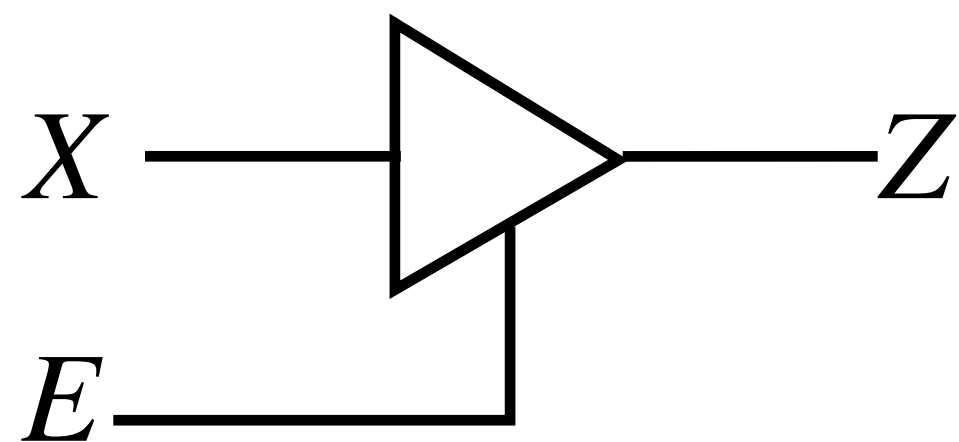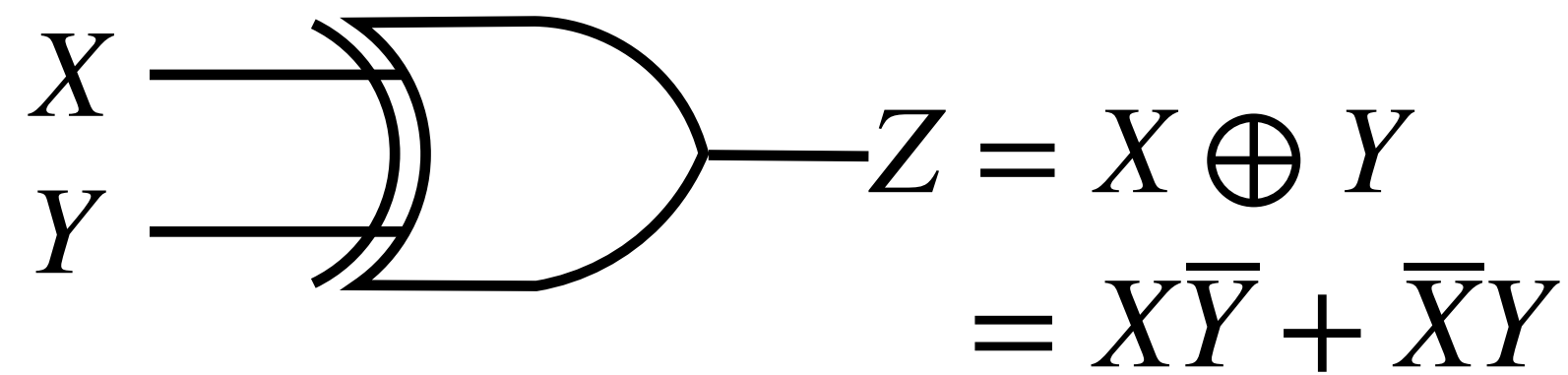
3-State Buffer

**XOR Gate
Exclusive-OR**

X

Y

$Z = X \oplus Y$

Buffer

X

$Z = X$

3-State Buffer

X

Z

E

3-State Buffer Truth Table

E	X	Z
0	0	Hi-Z
0	1	Hi-Z
1	0	0
1	1	1

Concept

XOR Gate

XOR Gate Exclusive-OR

$Z = X \oplus Y$
$= X\bar{Y} + \bar{X}Y$

XOR Truth Table

X	Y	$Z = X \oplus Y$
0	0	0
0	1	1
1	0	1
1	1	0

Concept

XOR Gate

- $X \oplus 0 = X$

- $X \oplus X = 0$

- $X \oplus \overline{Y} = \overline{X \oplus Y}$
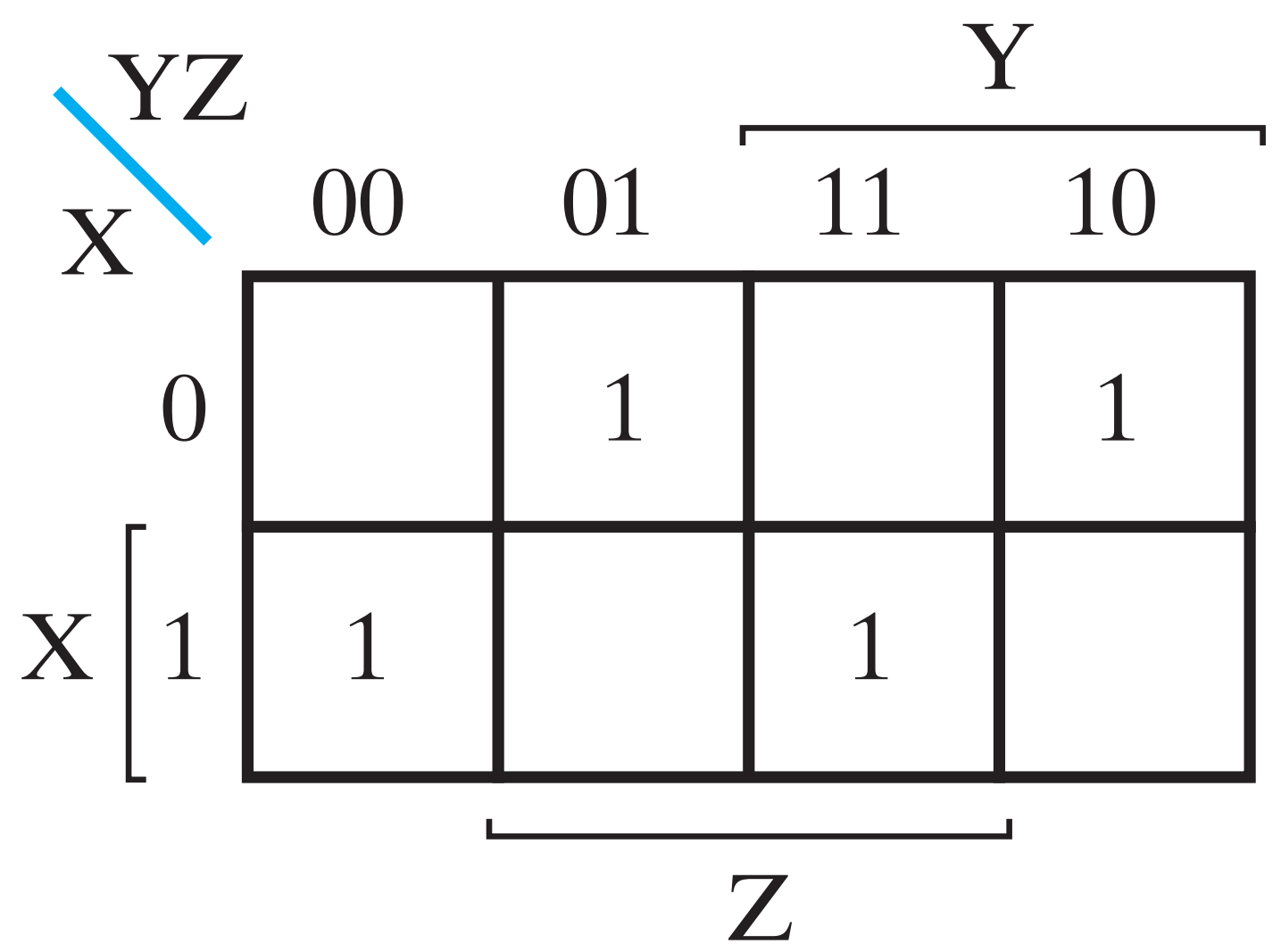
- $X \oplus 1 = \overline{X}$

- $X \oplus \overline{X} = 1$

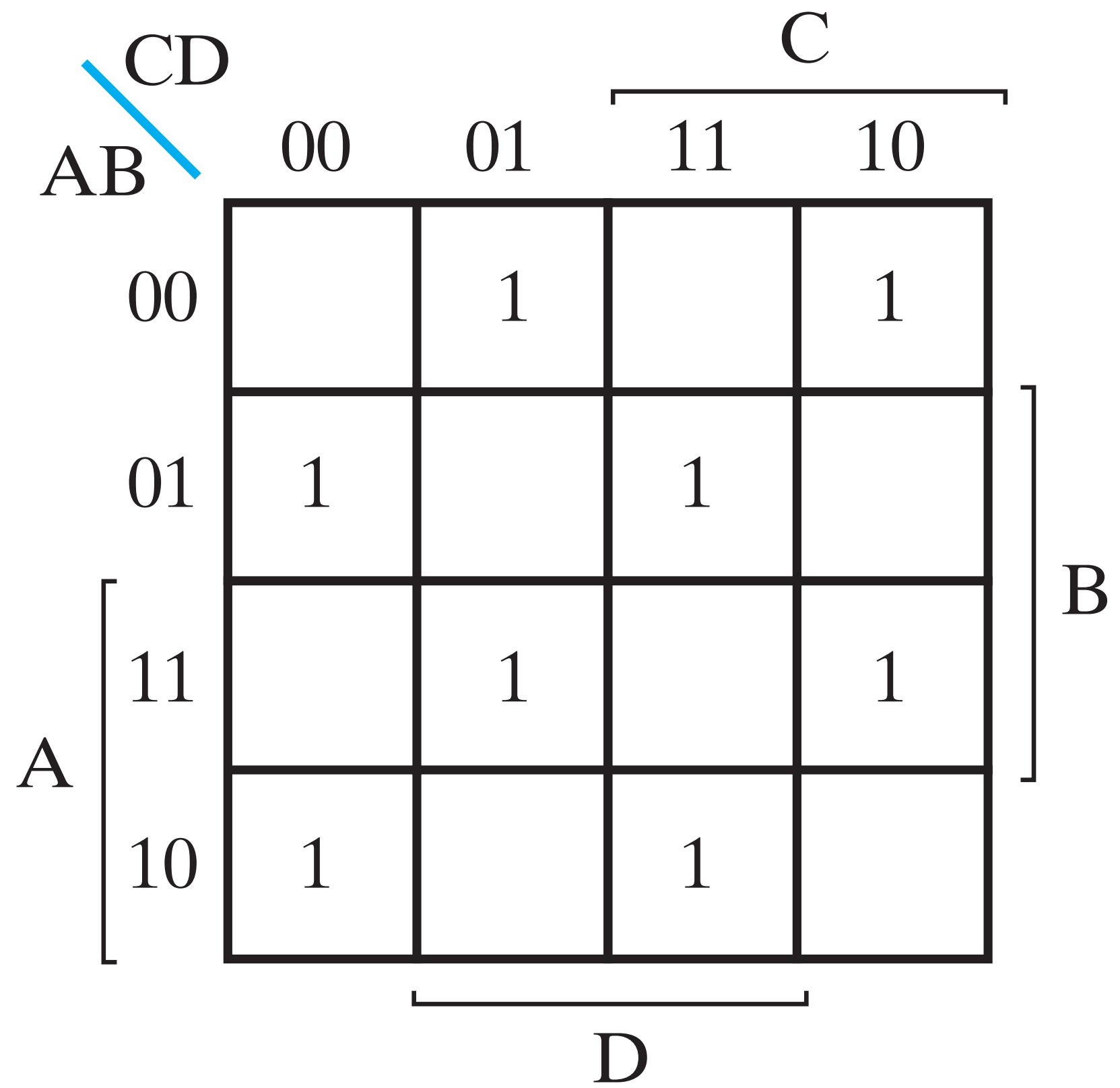- $\overline{X} \oplus Y = \overline{X \oplus Y}$

Odd and Even Functions

- Odd Functions

  - Outputs 1 if the **number of 1s** in the input is an **Odd** number

  - 2 variables: XOR

- Even Functions

  - Outputs 1 if the **number of 1s** in the input is an **Even** number

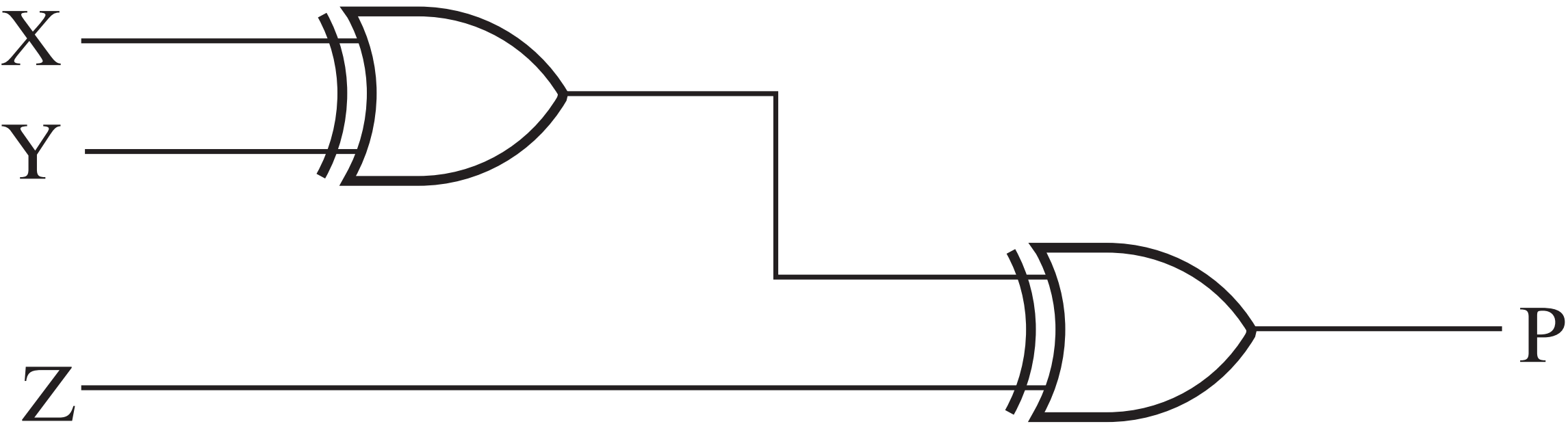 - 2 variables: XNOR

Concept
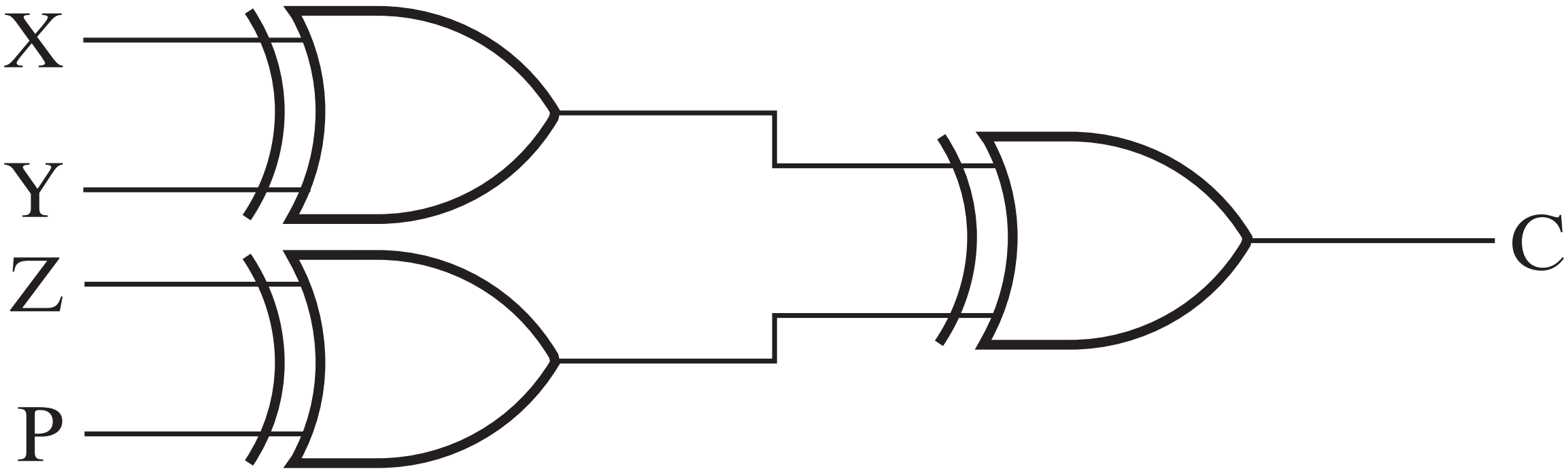
Odd Function K-Map

(a) $X \oplus Y \oplus Z$

(b) $A \oplus B \oplus C \oplus D$
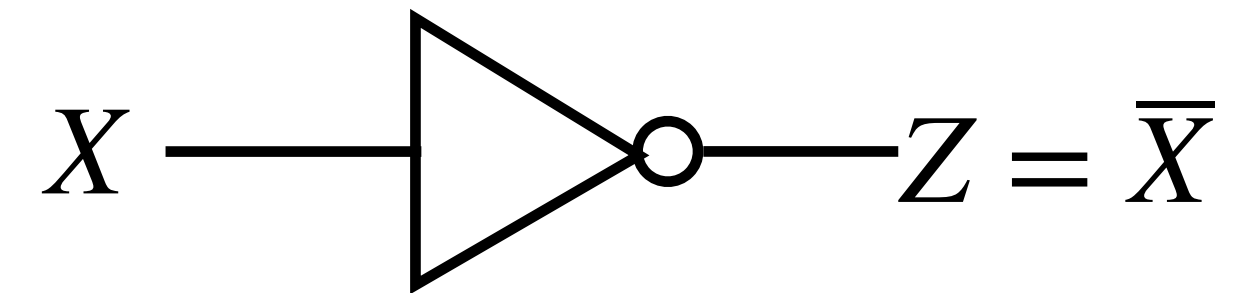
Odd Function Boolean Expressions

(a) $P = X \oplus Y \oplus Z$

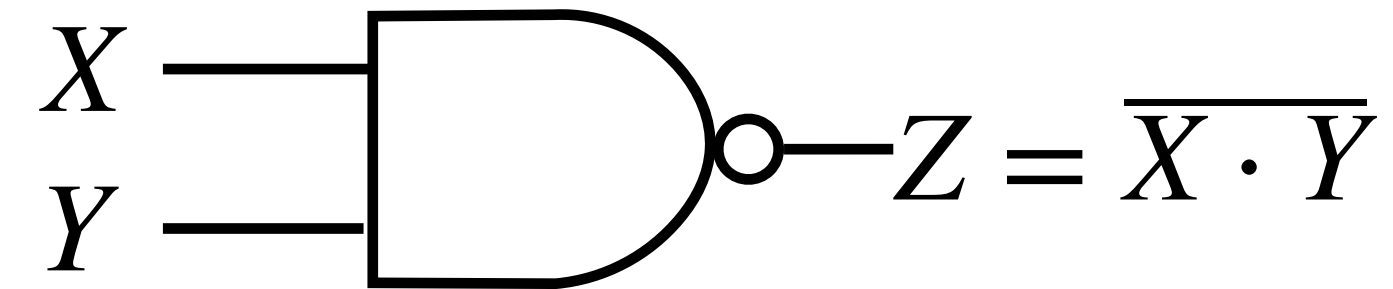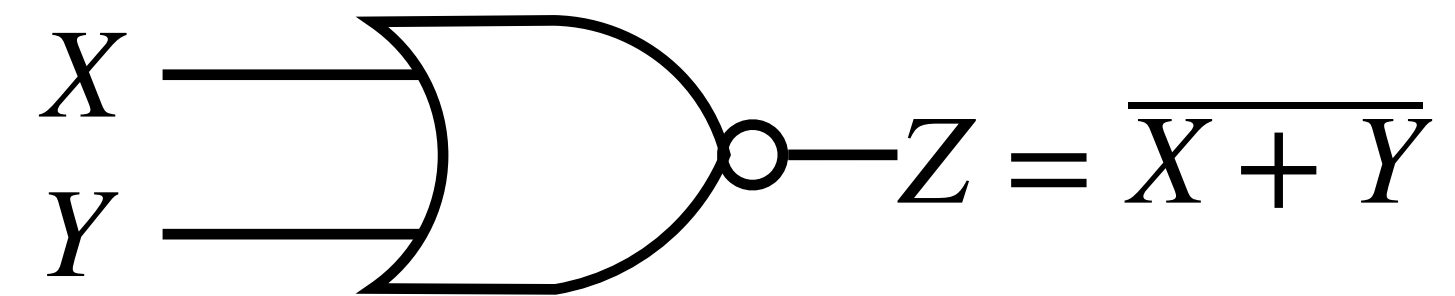(b) $C = X \oplus Y \oplus Z \oplus P$

Concept

N-Gates

NOT Gate X ——▷○—— $Z = \overline{X}$

NAND Gate $\begin{array}{c} X \\ Y \end{array}$ ——⊃○—— $Z = \overline{X \cdot Y}$

NOR Gate $\begin{array}{c} X \\ Y \end{array}$ ——▷○—— $Z = \overline{X + Y}$

XNOR Gate $\begin{array}{c} X \\ Y \end{array}$ ——▷○—— $Z = \overline{X \oplus Y}$
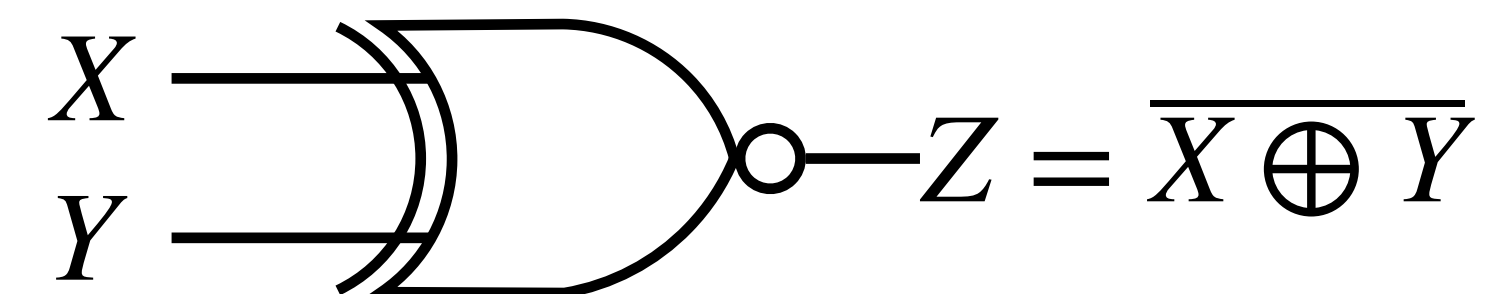
Summary

- Delay: Remember the Definitions!

  - Gate Delay and Propagation Delay

  - Transport and Inertial Delays

  - Standard Load

- Other Gates: Remember the Definitions!

  - XOR, Buffer, 3-State, NAND, NOR

Review